sddec18-20: High-Resolution ADC Using Delta-Sigma Architectures

Week 12 Report
April 16 - April 25

Team Members

Tyler Archer — *Test Lead Engineer*
Caleb Davidson — *Communications and Scribe Manager*
Caroline Alva — *Chief Engineer*
Mahmoud Gshash — *Meeting Facilitator*
Joshua Rolles — *Report Manager*

Summary of Progress this Report

Decimator was completed and tested with all the modulator and temperature sensor. Unit based testing has been completed. All components now in layout.

Pending Issues

Layout DRC did not match design as our design has pins that Encounter could not build. Will need to manually include those. In addition I had an issue where the design of the decimator would not import properly into Virtuoso in layout form, from Encounter. Simulations using our non-ideal clock runs very slow, resulting in long delays between sets of simulation results. This has prevented us from obtaining large sets of results. We plan to mitigate this problem going forward by running simulations on multiple machines simultaneously. Generally LVS and DRC issues that have been resolved.

Plans for Upcoming Reporting Period

Attach the circuit layout to the pad frame. Run post-layout simulations. Present on my findings in our presentation and work towards ensuring layout works as expected with post-layout simulations.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Tyler Archer	Completed final pre-layout testing of decimator connected to the modulator. Completed physical layout of remaining circuit blocks, and overall circuit.	23	123
Caleb Davidson	Found out the unit based model would run into similar issues that the full unit system would, but at the same time found the error in my full unit decimator filter. Once I found that issue I also could work through getting a layout from the synthesized code. Built that and testing the decimator from the verilog perspective.	16	98

Caroline Alva	I completed the layout and post layout simulations for the dynamic comparator. I edited and completed the Project Plan and I created the final presentation.	6	87
Mahmoud Gshash	Layout blocks for each of the digital designs made for the decimator.	15	88
Joshua Rolles	Redesigned the decimator, set up and ran several simulations to check functionality, changed verilog code for subcomponents of decimator, layout of subcomponents of the decimator structure	16	87