sddec18-20: High-Resolution ADC Using Delta-Sigma Architectures

Week 11 Report
April 9 - April 16

Team Members

Caleb Davidson — *Communications and Scribe Manager*
Joshua Rolles — *Report Manager*
Tyler Archer — *Test Lead Engineer*
Caroline Alva — *Chief Engineer*
Mahmoud Gshash — *Meeting Facilitator*

Summary of Progress this Report

Bringing all the portions of the ADC together. Finishing touches on the decimator design. Unit testing of functional blocks so as to verify design meets requirements.

Pending Issues

Issues with both versions of our decimator. Analog version is moving forward and will likely be close to layout. Verilog version has issues in porting to layout. Sizing constraints are being considered and might be an issue.

Plans for Upcoming Reporting Period

Look into sizing constraints. Verilog version get working in layout perspective. Analog version for decimator needs layout.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Caleb Davidson	Transitioned to a unit based Verilog design to ensure that our design will work with that to narrow down issues. Tried to see why synthesized Verilog does not look the same as unsynthesized Verilog.	15	82
Joshua Rolles	Imported decimator files into Cadence through Encounter RTL, set up test benches for decimator, ran several simulations on the decimator.	14	71
Tyler Archer	Integrated non-ideal comparator with modulator. Tested modulator with a variety of capacitor sizes. Finalized modulator schematic. Tested modulator with a variety of input voltages and confirmed proper functionality. Built layouts for the op amp and a few other blocks.	32	100

Caroline Alva	Designed a second dynamic comparator with low offset proposed in a paper co-authored by Professor Geiger. This circuit was compared with the double tail dynamic comparator circuit through simulation. Ultimately the double tail comparator was chosen based off of its simplicity.	5	81
Mahmoud Gshash	Put analog decimator together and make clock logic in analog form.	15	73