sddec18-20: High-Resolution ADC Using Delta-Sigma Architectures

Week 10 Report
April 2 - April 9

Team Members

Joshua Rolles — *Report Manager*
Caroline Alva — *Chief Engineer*
Tyler Archer — *Test Lead Engineer*
Caleb Davidson — *Communications and Scribe Manager*
Mahmoud Gshash — *Meeting Facilitator*

Summary of Progress this Report

Finish removing non-ideality error. Work through the combination of analog and digital components. Implement non-ideal components in a testbench ideal modulator circuit to identify and remove problems in non-ideal components.

Pending Issues

Using non-ideal components in the modulator leads to significant error. Importing the ideal modulator symbols into Cadence RTL errors. Different clocking signals between the mixed-signal design of our delta-sigma ADC. Because of various hardware limitations we need different clocks to time our input clock edge and output clock edges. Had difficulties opening the shared file of the ideal modulator.

Plans for Upcoming Reporting Period

The layout process of the dynamic comparator. Continue to import verilog into virtuoso and set up a test bench for the digital side of our circuit. Start RTL and Encounter transfer over from idealized Verilog to actual hardware. Fix error introduced by using non-ideal clock signals with the non-ideal DAC.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Joshua Rolles	Tested the ideal schematic with my DAC and it functions as expected. Imported Caleb's decimator and digital filter into RTL to form gate level schematic.	10	57
Caroline Alva	I have obtained a fully functional dynamic comparator. I have been building an ideal comparator to test against my dynamic comparator. I have also tested inside the ideal modulator to ensure that it results with as close to ideal results as possible.	10	76
Tyler Archer	Built and tested a new ideal switched capacitor DAC. Built and tested a new	16	68

	non-ideal switched capacitor DAC. Fixed problems with charge injection related to this DAC.		
Caleb Davidson	Finished building a decimator that simulates in Modelsim with multiple clocks, and all necessary design requirements.	12	67
Mahmoud Gshash	Built up a schematic decimator that works through unit testing. This will allow for multiple ways to implement the decimator so that we can have a fully functional design. Added reset and preset to DFF design.	8	58