sddec18-20: High-Resolution ADC Using Delta-Sigma Architectures

Week 9 Report
March 26 - April 2

Team Members

Caroline Alva — *Chief Engineer*
Caleb Davidson — *Communications and Scribe Manager*
Joshua Rolles — *Report Manager*
Tyler Archer — *Test Lead Engineer*
Mahmoud Gshash — *Meeting Facilitator*

Summary of Progress this Report

We are swapping our schematics with the ideal schematics of those circuits. Tried to test any components that are still running into issues, and try to verify that these issues are not related to non-idealities.

Pending Issues

Digital design does not implement as we have issues where the output is being driven low all the time. All signals are getting some value at this time though. The output voltage at the non-inverting terminal is producing an output that is desirable. Although the output voltage at the inverting terminal is producing an output that switches between 0 and several mV.

Plans for Upcoming Reporting Period

Continue swapping our schematics with the ideal schematics. Plan to test out different sizing techniques, and debugging the circuit to obtain a desirable output voltage at the inverting terminal. Resolve issue with output data. Change implementation to have different timing for clock signals.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Caroline Alva	I have built and simulated a Dynamic Comparator with three nmos switches and two latched stages allowing the signal to be latched either to VDD or VSS. I also placed buffers at each output made of four inverters.	11	66
Caleb Davidson	Issue where signal was being driven by two signals was fixed. Implemented different counter structure.	10	55
Joshua Rolles	Began swapping out ideal components from our ideal schematic with components we built. Tested DAC architecture within ideal modulator.	7	47

Tyler Archer	I continued testing the integrator and found capacitor sizes for the integrator and switched capacitor circuits that work well with each other. I also built a delta-sigma modulator using ideal components and performed simulations to ensure that it's behavior is ideal. This will be used to test other modulator components by substituting them for their ideal counterparts in the circuit.	9	52
Mahmoud Gshash	Building DFF from transistors and figuring out the right digital system to realize the Decimator from the building blocks I made last week. Schematic form of a decimator being built.	8	50