

**sddec18-20: High-Resolution ADC Using Delta-Sigma Architectures**

Week 8 Report

March 19 - March 26

**Team Members**Caleb Davidson — *Communications and Scribe Manager*Joshua Rolles — *Report Manager*Tyler Archer — *Test Lead Engineer*Caroline Alva — *Chief Engineer*Mahmoud Gshash — *Meeting Facilitator***Summary of Progress this Report**

Design changes based on new information, and changing requirements for functionality. We have been able to understand what needs to be changed, and start in the alteration process.

**Pending Issues**

Different design requirement than was originally envisioned for digital filtration system.

**Plans for Upcoming Reporting Period**

Need to restart on the Verilog to build the new filtration system. Errors in design on the analog side will need to be changed based on current issues, and changes in design requirements. The testing for constant components will need to be worked through and properly tested fully.

**Individual Contributions**

Team Member	Contribution	Weekly Hours	Total Hours
Caleb Davidson	Started on averaging filter design. Built a basic design in Modelsim and looked at what previous units have been built from past classes that would be used in this design.	8	45
Joshua Rolles	Worked on low pass filter code and decimator code personally.	4	40
Tyler Archer	I worked on writing testing plans for the integrator and for the overall ADC circuit, which will be part of version 2 of our project plan. I also completely redesigned the op amp that we are using for the temperature sensor and the integrator to work with a 0V-1.8V voltage range.	9	43
Caroline Alva	I have simulated the conventional dynamic comparator and analyzed the results. The	8	55

