sddec18-20: High-Resolution ADC Using Delta-Sigma Architectures

Week 7 Report
March 5 - March 19

Team Members

Caleb Davidson — *Communications and Scribe Manager*
Joshua Rolles — *Report Manager*
Caroline Alva — *Chief Engineer*
Tyler Archer — *Test Lead Engineer*
Mahmoud Gshash — *Meeting Facilitator*

Summary of Progress this Report

Finished basic testing of unit components. Tried to start connecting components in a logical progression. Some issues arose in the current implementation that need to adjust the structure so we will need to go back to designing some components.

Pending Issues

Characteristics of the technology file were brought to light that changes our design at a fundamental level. The voltage swing is EITHER 0 to 1.8V or -0.9 to 0.9 V. Two stage op amp will not sufficiently work in the context of a comparative ADC circuit.

Plans for Upcoming Reporting Period

Revise current designs to work within the realms of these new characteristics. If needed start over on any circuits that will not fit what was originally expected.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Caleb Davidson	Started Verilog implementation of the Sinc1 filtration system. Built a basic design and testbench, but the clocking is off. The clocking will need to be carefully diagrammed out because that will determine whether the design functions properly or not.	8	37
Joshua Rolles	Met with Caleb to discuss plans for the digital filter and decimator. Researched sinc1 and sinc3 filters. Compared performance between different low pass filters for our design. Viewed other decimators available to learn their purpose.	6	36
Caroline Alva	I have researched in the IEEE journals dynamic comparator designs and their	9	47

	functionalities. I have been comparing characteristics to find a design that would work best inside our delta sigma modulator. Focus on the documentation of design and testing of my comparator.		
Tyler Archer	I assembled the integrator using the op amp, a capacitor, and two switched capacitor circuits. I simulated the circuit with a variety of inputs and attempted to size the capacitors so that the circuit behaved as we need it to.	8	34
Mahmoud Gshash	Testing the functionality of the bootstrapped circuit with the switch capacitor circuits. Found quantization errors and overshoots.		37