sddec18-20: High-Resolution ADC Using Delta-Sigma Architectures

Week 6 Report
February 26 - March 5

Team Members

Caleb Davidson — *Communications and Scribe Manager*
Caroline Alva — *Chief Engineer*
Joshua Rolles — *Report Manager*
Mahmoud Gshash — *Meeting Facilitator*
Tyler Archer — *Test Lead Engineer*

Summary of Progress this Report

Implementation ran into errors and issues with analog circuit design. As we try to build the structure more non-idealities are creeping in. Started testing to try and find any issues in the current design.

Pending Issues

Unsure of what simulations would be necessary to ensure that the comparator was sufficiently designed. Bootstrapping switch does not run as expected. Decimator has a multiple drivers issue.

Plans for Upcoming Reporting Period

Fix errors in non-idealities, and ensure testplan is fleshed out for each component on a unit level.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Caleb Davidson	Tried to implement using a Sinc filter, but this seems to maybe not work with the way we are implementing the rest of the circuit. Worked through what a design on pen and paper would look like for Sinc1 and Sinc3.	6	29
Caroline Alva	I designed and simulated a two stage operational amplifier-based comparator. The comparator is fully functional as far as testing has currently shown.	8	38
Joshua Rolles	Tested the 1-bit DAC with a transient response for different input signals and different reference voltages to verify functionality with multiple reference voltages.	6	30
Mahmoud Gshash	Bootstrapping switch was able to be initially tested to work. This is only based on initial	10	37

	testing. Some issues still seem present, and the structure was decided between inverting and non-inverting.		
Tyler Archer	I completed building and testing the schematic for the op amp that will be used for the integrator.		26