sddec18-20: High-Resolution ADC Using Delta-Sigma Architectures

Week 5 Report
February 19 - February 26

Team Members

Tyler Archer — *Test Lead Engineer*
Joshua Rolles — *Report Manager*
Caroline Alva — *Chief Engineer*
Caleb Davidson — *Communications and Scribe Manager*
Mahmoud Gshash — *Meeting Facilitator*

Summary of Progress this Report

Started implementation of designs by building schematics for most components on the transistor/logic perspective.

Pending Issues

For filtration there is some question of what the exact cut off frequency and components of the filter will look like. Transient response of the dynamic comparator circuit does not simulate as expected so will need to investigate the characteristics causing this.

Plans for Upcoming Reporting Period

Continued progress in implementation in written schematics. Start taking schematics drawn out and moving them onto computational modeling (Cadence).

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Tyler Archer	I worked on building an op amp schematic. I also researched bootstrapping for the switched capacitor circuit.	8	26
Joshua Rolles	Designed the 1-bit DAC schematic, performed simulations for the DAC, researched digital filter and decimator designs	8	24
Caroline Alva	Worked through planning out the next week in terms of what each member should be accomplishing, as well as assessing where we currently stand in the progress.	4	30
Caleb Davidson	Started implementation of the digital side filtration. This is currently being done using a digital low-pass filter made up of a moving set of impulse responses summed together. In	8	23

	the decimation side currently it seems like the data will be stored and only one of the many data points will be used for the output value.		
Mahmoud Gshash	Switch capacitor circuit implementation with experimentation of different architectures. Tried to look into inverting and non-inverting structures.	8	27