sddec18-20: High-Resolution ADC Using Delta-Sigma Architectures

Week 4 Report
February 11 - February 18

Team Members

Tyler Archer — *Test Lead Engineer*
Caroline Alva — *Chief Engineer*
Joshua Rolles — *Report Manager*
Mahmoud Gshash — *Meeting Facilitator*
Caleb Davidson — *Communications and Scribe Manager*

Summary of Progress this Report

Started progress on individual unit designs. Looked into the various types of implementations to decide which would be a best fit. Introduced tool flow decisions and made the decision to utilize Cadence Virtuoso with potentially Verilog as an HDL tool choice for digital design.

Pending Issues

-I have had some difficulty determining the correct technology file to use in Cadence Virtuoso for the 180 nm process.
-The comparator functionality
-I had issues with understanding the bootstrapping switch for the sample and hold circuit
-Design requirements for the implementation of the filtration systems

Plans for Upcoming Reporting Period

Continue progress of individual unit design phase. Report on progress and coordinate how all members' components will integrate. Unit testing to start in the next period as well.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Tyler Archer	I experimented with telescopic cascode op amp designs to attempt to find a design strategy that will allow 0V quiescent input and output.	5	18
Caroline Alva	Created using Cadence a simple comparator using a two stage amplifier. Simulated the circuit to ensure that it functioned as a comparator	12	26
Joshua Rolles	Researched DAC architectures, looked into sizing strategies for transmission gates, imported the 180 nm technology file into cadence	4	16

Mahmoud Gshash	Researched a simple bootstrapped switch circuit that meets the requirement for our project	7	19
Caleb Davidson	Ensured various members components was split properly. Tried to figure out what low pass characteristics were needed for the low-pass filter. Looked into different implementations of the low pass filter (convolution in time using integrated approach, convolution using a digital approach, RC characteristic, active vs. passive, etc.).	4	15