sddec18-20: High-Resolution ADC Using Delta-Sigma Architectures

Week 3 Report
February 4 - February 11

Team Members

Tyler Archer — *Test Lead Engineer*
Joshua Rolles — *Report Manager*
Caroline Alva — *Chief Engineer*
Caleb Davidson — *Communications and Scribe Manager*
Mahmoud Gshash — *Meeting Facilitator*

Summary of Progress this Report

Continued research progress specific to the components that each member would be building in the future. Split up work according to what each member would like to work on. Work on a technical nature came through pen and paper schematic drawings.

Pending Issues

No pending issues in design. Still working out building up communication protocols and how to gather data. Dr. Geiger will be gone, and so we will need to setup alternative times to meet.

Plans for Upcoming Reporting Period

Start the design process with current information to start working towards a rev. 1 design. Each member should be working on their individual component.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Tyler Archer	I researched operational amplifier structures and evaluated them on their suitability for use in our project. Used a model-based approach to do this.	5	13
Joshua Rolles	Continued research on ADCs, decimators, and switched capacitor filters, reviewed/edited the project plan. Pen and paper implementation has been started.	4	12
Caroline Alva	Researched comparator circuits for the 1 bit ADC. I created the outline for the project.	4	14
Caleb Davidson	Implemented a google form to allow for easier access to update information from all group members. In addition worked on looking into the digital filter and decimater	3	11

	and see what would be best as a viable option for me to work on. Finally updated team members on weekly meeting notes, and collected that data in an easy to use system.		
Mahmoud Gshash	I started researching bootstrap switch capacitor to be used in our filter. There were several papers that propose a high-speed high-linearity schematics with different complexity. Therefore, I am in the phase of implementing the schematics and test their performance to further understand the circuit and make the right discussion on which design will best fit our purposes.	4	12