

## sddec18-20: High-Resolution ADC Using Delta-Sigma Architectures

Week 2 Report

January 28 - February 4

### Team Members

Caroline Alva — *Chief Engineer*

Caleb Davidson — *Communications and Scribe Manager*

Tyler Archer — *Test Lead Engineer*

Joshua Rolles — *Report Manager*

Mahmoud Gshash — *Meeting Facilitator*

### Summary of Progress this Report

Built up a more adequate knowledge base about the architecture and device we will be constructing. Worked through verifying details of the project, and dividing some portions of the project to various members. We set forth what the different design specifications for the overall unit will need to be (input and output, temperature and data output). Specifically we set which members would be in charge of which managerial duties in the group.

### Pending Issues

Issues revolve around next steps. Mainly we are struggling with some details of how to do reporting, updates, and tracking of documentation. As well we are trying to assign workloads among all members evenly without much conflict.

### Plans for Upcoming Reporting Period

We are trying to verify which people are going to be working on what subsystems of this larger project base. In addition we are working towards presenting the research and design requirements we have collected so far to Dr. Geiger.

### Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Caroline Alva	I researched switched capacitor integrator circuits, to gain a better understanding of it's part in the delta sigma modulator. I researched comparators circuits that would be equivalent to a 1-bit ADC, and circuits that can be used for the 1-bit DAC. I also researched which type of operational amplifier would work best for each circuit. I read several papers in the IEEE symposium of circuits and systems, regarding high resolutions data converters.	6	10

