EE/CprE/SE 492 BI-WEEKLY REPORT 6 11/6 – 11/19

Group number: sddec18-20

Project title: Delta Sigma ADC

Client &/Advisor: Randall Geiger and Degang Chen

Team Members/Role:

Tyler Archer — Test Lead Engineer

Caleb Davidson — Communications and Scribe Manager

Caroline Alva — Chief Engineer

Mahmoud Gshash — Meeting Facilitator

Joshua Rolles — Report Manager

Weekly Summary

Finalizing test plan work and confirmed the code for testing as well as initial design of a PCB for the testing of our device. Schematic design is mostly complete, and now we are trying to get software setup for the process we are designing in for layout.

Past week accomplishments

- **Tyler Archer:** Worked with ETG to get Calibre enabled for Cadence. Obtained rule file locations from UT Dallas. Tried some test layouts, ran Calibre DRC and identified a problem with 2.5V transistors being recognized as 3.3V by Calibre. Worked with ETG and students experienced with 65nm process to try to fix the problem.
- **Mahmoud Gshash:** Finished level shifters schematics and testbench. In addition, finished half of the digital component of the decimation unit. Some parts did not the expected output; therefore, it has to be revised later.
- **Caroline Alva:** Wrote code for the tests to be conducted for the ADC
- **Josh Rolles:** Researched INL and DNL per Dr. Geiger's request to add these characterizations to the test plan.
- **Caleb Davidson:** Worked on PCB design for a test bed for future testing. Worked with Caroline and Josh to finalize the test plan and got feedback from Dr. Geiger on our current progress.

Pending issues

- Tyler Archer: We need to determine what resistors to use, and what pad cells to insert into the pad frame. We need a startup circuit for the temperature sensor. We need to complete top-level schematics and test them. We need to fix DRC issues and make sure correct rule files are being used and necessary permissions are set.
- Mahmoud Gshash: Starting layout for additional part and figuring out Caliber design rules the creates design rule violations.
- Caroline Alva: No issues
- Josh Rolles: INL and DNL aren't typically reported for ADCs because of the way the converter outputs new codes.
- Caleb Davidson: Testplan needs some tweaking as we have need to consider some more test scenarios.

Individual contributions

Name	Individual Contributions	Hour Worked	Cumulative Hours Worked
Tyler Archer	• Worked with ETG to get Calibre enabled for Cadence. Obtained rule file locations from UT Dallas. Tried some test layouts, ran Calibre DRC and identified a problem with 2.5V transistors being recognized as 3.3V by Calibre. Worked with ETG and students experienced with 65nm process to try to fix the problem.	6	55
Mahmoud Gshash	• Finished level shifters schematics and testbench. In addition, finished half of the digital component of the decimation unit. Some parts did not the expected output; therefore, it has to be revised later.	12	40

Caroline Alva	• Creating the final poster and working on the final report	4	27
Josh Rolles	• Researched INL and DNL per Dr. Geiger's request to add these characterizations to the test plan.	4	29
Caleb Davidson	• Ensured the DAQ meets the specification for our test plan for our design. Met up with Caroline and Josh separately to work through verifying that the test plan can be merged together and the testing will work. Started schematics for a PCB design.	10	34

Plans for the upcoming week

- Tyler Archer: We plan to complete top-level schematics, test them, and complete all layouts by the end of this week. We plan to do post-layout simulations and insert our circuit in a pad frame next week.
- Mahmoud Gshash: Finishing schematics and starting layout.
- Caroline Alva: Making the last minute adjustments to the final report.
- Josh Rolles: Assist with final report preparation and begin to prepare for the IRP presentation.
- Caleb Davidson: Add additional test procedures from feedback provided from Dr. Geiger. Fix PCB to match what our design changes are as of right now.