EE/CprE/SE 492 BI-WEEKLY REPORT 5 10/23 – 11/5

Group number: sddec18-20

Project title: Delta Sigma ADC

Client &/Advisor: Randall Geiger and Degang Chen

Team Members/Role:

Tyler Archer — Test Lead Engineer

Caleb Davidson — Communications and Scribe Manager

Caroline Alva — Chief Engineer

Mahmoud Gshash — Meeting Facilitator

Joshua Rolles — Report Manager

Weekly Summary

In our design we have redesigned the majority of the circuitry schematics to the 65 nm technology specifications. From a testing perspective we met to verify that the testplan can be merged correctly between our different writing styles.

Past week accomplishments

- **Tyler Archer:** Designed, built, and tested schematics for the temperature sensor, bias current generator, and capacitor blocks. Split the analog supplies into two separate ones to avoid switching noise showing up on the op amp and temperature sensor supplies. Researched capacitor options and identified one that will work. Laid out capacitors.
- **Mahmoud Gshash:** Gained access to the new process and decided what devices we are using for digital and analog parts. We will use 1.1V transistors for digital parts and 2.5V transistors for analog parts.
- **Caroline Alva:** Researched the tests needed to be run on the ADC from looking at datasheets of ADCs on the market.
- **Josh Rolles:** Further research done on SNR, SNDR, ENOB to ensure that the steps and equations used in the test plan were accurate for the Delta Sigma architecture.
- **Caleb Davidson:** Ensured the DAQ meets the specification for our test plan for our design. Met up with Caroline and Josh separately to work through verifying that the test plan can be merged together and the testing will work. Started schematics for a PCB design.

Pending issues

- Tyler Archer: We need to determine what resistors to use, and what pad cells to insert into the pad frame. We also need to determine how to correctly lay out transistors in this dual-well process. We need to verify what options are available for our process run to make sure all features used in our design are available. We need to see if we can add more pins to the pad frame and whether we need a startup circuit for the temperature sensor.
- Mahmoud Gshash: Finishing level shifters schematic and testbenches.
- Caroline Alva: No issues continuing to work on the code for the characterization of the ADC.
- Josh Rolles: None
- Caleb Davidson: Need to finalize that our DAQ and potential PCB design will fit our needs.

Individual contributions

Name	Individual Contributions	Hour Worked	Cumulative Hours Worked
Tyler Archer	● Designed, built, and tested schematics for the temperature sensor, bias current generator, and capacitor blocks. Split the analog supplies into two separate ones to avoid switching noise showing up on the op amp and temperature sensor supplies. Researched capacitor options and identified one that will work. Laid out capacitors.	15	49
Mahmoud Gshash	● Gained access to the new process and decided what devices we are using for digital and analog parts. We will use 1.1V transistors for digital parts and 2.5V transistors for analog parts.	8	28
Caroline Alva	● Wrote code for the tests to be	5	23

	conducted for the ADC		
Josh Rolles	• Further research done on SNR, SNDR, ENOB to ensure that the steps and equations used in the test plan were accurate for the Delta Sigma architecture.	4	25
Caleb Davidson	• Ensured the DAQ meets the specification for our test plan for our design. Met up with Caroline and Josh separately to work through verifying that the test plan can be merged together and the testing will work. Started schematics for a PCB design.	4	24

Plans for the upcoming week

- Tyler Archer: Complete schematics for analog and top-level schematic simulation for analog and digital. Complete layout for analog and post-layout simulation for analog and digital.
- Mahmoud Gshash: Finishing schematics and testbench for level shifters and starting the schematics of the digital parts.
- Caroline Alva: Continue working on the test plan and developing code also creating the final poster.
- Josh Rolles: Continue to update my portion of the test plan to ensure accuracy
- Caleb Davidson: Complete PCB design schematic and move to drawing traces. Finish the testplan merging process. Ensure the testplan meets all requirements.