EE/CprE/SE 492 BI-WEEKLY REPORT 4 10/8 – 10/22

Group number: sddec18-20

Project title: Delta Sigma ADC

Client &/Advisor: Randall Geiger and Degang Chen

Team Members/Role:

Tyler Archer — Test Lead Engineer

Caleb Davidson — Communications and Scribe Manager

Caroline Alva — Chief Engineer

Mahmoud Gshash — Meeting Facilitator Joshua Rolles — Report Manager

Weekly Summary

In terms of design, we built and tested the large majority of the changes from our previous design. We also connected with graduate students in order to interface with the challenges that this new design will bring. Wrapped up the test plan process, and decided on a DAQ system that will work for our device for initial testing.

Past week accomplishments

- **Tyler Archer: Designed and tested schematics for a folded cascode amplifier for use in the integrator and temperature sensor. Designed as tested switched capacitor circuits, integrator, DAC, comparator, pulser, and 2.5V DFF. Used these blocks to build and test the modulator schematic. Sized modulator capacitors and obtained test results showing error at the 1 part per 1000 level which is satisfactory. Obtained pad frame.**
- **Mahmoud Gshash:** Signed NDA form and discussed new process with team members.
- **Caroline Alva:** Looked into the test plan for delta-sigma data converters the manner in which necessary to extract the spectral characteristics is different for this architecture than the other architectures. I also began setting up the 65nm process to create the 1-bit ADC
- **Josh Rolles: Finished my portion of the test plan in one document. This plan will eventually be implemented with Caroline and Caleb's portions as well to create a complete test plan for the ADC.**
- **Caleb Davidson: Detailed my portion of the test plan into easy to digest segments, and logical order. Decided on a DAQ system that would be adequate for initial testing. Wrote out initial thoughts on how DAQ will be used in our test plan. Researched how the DAQ would be used in our system, and which DAQ will fit into our needs.**

Pending issues

- Tyler Archer: The model numbers of the IC package and socket we will use need to be determined. We plan to use the same one that other students are using for fabrication in this process, but information from them hasn't been clear so far. This needs to be determined because it may affect how the pad frame needs to be laid out.
- Mahmoud Gshash: *Waiting for gaining access to the new process and understanding the available devices.*
- Caroline Alva: Working on the outline and retrieving information for the tests to be ran on the fabricated ADC

- ➢ Josh Rolles: Need to meet with Caroline and Caleb to consolidate our portions of the test plan into one complete document. This should be done within the next few days and able to be inserted into our final design document.
- ➢ Caleb Davidson: Meeting setup with Josh and Caroline to update the test plan as one coherent document. Then implementing that into the final design document. We have had some sickness, and general availability issues to get the meeting setup.

Individual contributions

Name	Individual Contributions	Hour Worked	Cumulative Hours Worked
Tyler Archer	• Designed and tested schematics for a folded cascode amplifier for use in the integrator and temperature sensor. Designed as tested switched capacitor circuits, integrator, DAC, comparator, pulser, and 2.5V DFF. Used these blocks to build and test the modulator schematic. Sized modulator capacitors and obtained test results showing error at the 1 part per 1000 level which is satisfactory. Obtained pad frame.	22	34
Mahmoud Gshash	• Waiting for gaining access to the new process and understanding the available devices.	• 8	• 20
Caroline Alva	• Reviewing data sheets for the ADC to find the most appropriate procedure to test the ADC	• **4**	• **15**

Josh Rolles	• **Finished my portion of the test plan in one document. This plan will eventually be implemented with Caroline and Caleb's portions as well to create a**	6	21
	complete test plan for the ADC.		
Caleb Davidson	• **Detailed my portion of the test plan into easy to digest segments, and logical order. Decided on a DAQ system that would be adequate for initial testing. Wrote out initial thoughts on how DAQ will be used in our test plan. Researched how the DAQ would be used in our system, and which DAQ will fit into our needs.**	8	20

Plans for the upcoming week

- ➢ Tyler Archer: Design and test schematics for the temperature sensor and pad frame. Compile schematics for complete ADC and run simulations. Begin work on analog block physical layouts. Obtain information on voltage and current references needed for testing. Obtain information on IC package and socket to prepare for the PCB design.
- ➢ Mahmoud Gshash: *Start schematics for building and testing level shifters.*
- ➢ Caroline Alva: Continue working on the test plan and developing code to create the characteristic analysis
- ➢ Josh Rolles: Consolidate all 3 separate testing plans into one complete document and add it to the final design document. Once this is done, I will plan on assisting with any layout tasks that may need to be done.
- ➢ Caleb Davidson: Meeting setup with Josh and Caroline to update the test plan as one coherent document. Then implementing that into the final design document. Update test plan with changes due to DAQ change.