EE/CprE/SE 492 BI-WEEKLY REPORT 3 9/18 – 10/1

Group number: sddec18-20

Project title: Delta Sigma ADC

Client &/Advisor: Randall Geiger and Degang Chen

Team Members/Role:

Tyler Archer — Test Lead Engineer

Caleb Davidson — Communications and Scribe Manager

Caroline Alva — Chief Engineer

Mahmoud Gshash — Meeting Facilitator

Joshua Rolles — Report Manager

Weekly Summary

Starting to transition to building our design in the 65nm process. As some members start that effort, the rest will be working on finishing up the test plan and documentation. Some progress on both of these paths has been accomplished.

Past week accomplishments

- **Tyler Archer:** Spoke to an engineer at Texas Instruments who works in Cadence product support and determined that it would take more work to convert the USMC 0.18um design to the native TSMC 0.18um process than it would take to create a new design for the 65nm process. Installed UMC 65nm process technology files for Cadence. Read through 65nm process documentation and identified MOS and BJT components that could be used for our design. Created a testing schematic and extracted values of uCox and Vth for PMOS and NMOS devices.
- **Mahmoud Gshash:** We found out that the team does not have access to the process-native files. Therefore, we are considering to start-over in a new process (65 nm).
- **Caroline Alva:** Looked into the test plan for delta-sigma data converters the manner in which necessary to extract the spectral characteristics is different for this architecture than the other architectures. I also began setting up the 65nm process to create the 1-bit ADC
- **Josh Rolles: Researched various spectral and behavioral characteristics for ADCs. Read many data sheets and articles about proper testing of the Delta-Sigma architecture testing.**
- **Caleb Davidson:** Updated my test plan with proposed ideas, and presented a few during our current meetings. Set up a draft copy of the test plan so as to provide updates in the future. Looked into a few types of data acquisition equipment we could use for our design.

Pending issues

- Tyler Archer: I need to research the available resistor types and find out what layers in the 65nm process we may be restricted from using.
- Mahmoud Gshash: Waiting for advisor to get the NDA form of the new process.
- Caroline Alva: Researching the 65nm process, to obtain the parameters of this process to further create designs.
- Josh Rolles: Test plan needs to be completed and compiled from other group members.
- Caleb Davidson: Test plan is currently not in a ready state. Uncertainty on the viability of some of the test equipment (particularly the NI data acquisition system).

Individual contributions

Name	Individual Contributions	Hour Worked	Cumulative Hours Worked
Tyler Archer	• Spoke to an engineer at Texas Instruments who works in Cadence product support and determined that it would take more work to convert the USMC 0.18um design to the native TSMC 0.18um process than it would take to create a new design for the 65nm process. Installed UMC 65nm process technology files for Cadence. Read through 65nm process documentation and identified MOS and BJT components that could be used for our design. Created a testing schematic and extracted values of uCox and Vth for PMOS and NMOS devices.	4	12
Mahmoud Gshash	• We found out that the team does not have access to the process-native files. Therefore, we are considering to start-over in a new process (65 nm).	4	12
Caroline Alva	• Looked into the test plan for delta-sigma data converters the manner in which necessary to extract	4	

	the spectral characteristics is different for this architecture than the other architectures. I also began setting up the 65nm process to create the 1-bit ADC		
Josh Rolles	• Researched various spectral and behavioral characteristics for ADCs. Read many data sheets and articles about proper testing of the Delta-Sigma architecture testing.	8	15
Caleb Davidson	• Updated my test plan with proposed ideas, and presented a few during our current meetings. Set up a draft copy of the test plan so as to provide updates in the future. Looked into a few types of data acquisition equipment we could use for our design.	4	12

Plans for the upcoming week

- Tyler Archer: I plan to extract values of lambda for NMOS and PMOS in the 65nm process, or at least determine at what device length lambda begins to significantly level off, create a list of needed project design components, and design an opamp for the integrator and temperature sensor.

- Mahmoud Gshash: Sign NDA and start building Schematics.
- Caroline Alva: Continue working on the 65nm process and finish simulating the 1-bit ADC.
- Josh Rolles: No report received
- Caleb Davidson: Look at the design document from last semester and look into integrating my test plan with that. Update my test plan to look more professional, and be laid out better.