EE/CprE/SE 492 BI-WEEKLY REPORT 2 9/11 – 9/24

Group number: sddec18-20

Project title: Delta Sigma ADC

Client &/Advisor: Randall Geiger and Degang Chen

Team Members/Role:

Tyler Archer — Test Lead Engineer

Caleb Davidson — Communications and Scribe Manager

Caroline Alva — Chief Engineer

Mahmoud Gshash — Meeting Facilitator

Joshua Rolles — Report Manager

Weekly Summary

.

Past week accomplishments

- **Tyler Archer: Contacted six professors and a PHD student at Texas A&M to attempt to find resources for doing CMP density and antenna rule checks. Researched SCMOS rules and their suitability for creating IC designs for fabrication. Determined that the SCMOS rules used for our design are no longer allowed for fabrication through MOSIS. Researched UMC 65nm process, which we plan to attempt to move our design to. Signed and returned NDA for 65nm process. Researched ADC specifications and testing.**
- **Mahmoud Gshash: Determined that the files installed in cadence are generic files and original files are required to send the spring design to the foundry.**
- **Caroline Alva: Studied and researched best possible ways to determine spectral characteristics of the ADC; specifically focused on gain error, offset error and full scale error. Began to determine a baseline testbench to find these possible errors in the ADC.**
- **Josh Rolles: Researched standard ways to determine spectral characteristics to characterize our ADC, specifically ENOB, INL, DNL, SNDR, SNR. Determined the most efficient approach to evaluating these characteristics for the delta-sigma architecture.**
- **Caleb Davidson: Created an initial test plan for my portion of the tests. Defined what the tests would look like. Gave example test strategies and outputs.**

Pending issues

- Tyler Archer: I need access to UMC 65nm design rules and process features description to see how much changing is guaranteed to have to be done to our design to move it to this process.
- Mahmoud Gshash: Find where we can get the process-native files to run the design rule checks on the current design and find out if there are any violations that need to be fixed before sending the design to the foundry.
- Caroline Alva: I will continue to work on the testbench, but I will also be waiting to hear what changes need to be made when moving to the 65nm process.
- Josh Rolles: Continue to work on the test bench and assist with the 65nm transition if issues arise.

➢ Caleb Davidson: Need to alter my test plan from the feedback I received during our meeting. Changes with regard to the 65nm process. Need clarity on the length/verbosity of the test plan for my individual tests.

Individual contributions

Name	Individual Contributions	Hour Worked	Cumulative Hours Worked
Tyler Archer	• Contacted six professors and a PHD student at Texas A&M to attempt to find resources for doing CMP density and antenna rule checks. Researched SCMOS rules and their suitability for creating IC designs for fabrication. Determined that the SCMOS rules used for our design are no longer allowed for fabrication through MOSIS. Researched UMC 65nm process, which we plan to attempt to move our design to. Signed and returned NDA for 65nm process. Researched ADC	4	8

	specifications and testing.		
Mahmoud Gshash	● Determined that the files installed in cadence are generic files and original files are required to send the spring design to the foundry.	4	8
Caroline Alva	● Studied and researched best possible ways to determine spectral characteristics of the ADC; specifically focused on gain error, offset error and full scale error. Began to determine a baseline testbench to find these possible errors in the ADC.	3	7
Josh Rolles	● Researched standard ways to determine spectral characteristics to characterize our ADC, specifically ENOB, INL, DNL, SNDR, SNR. Determined the most efficient	3	7

	approach to evaluating these characteristics for the delta-sigma architecture		
Caleb Davidson	• Created an initial test plan for my portion of the tests. Defined what the tests would look like. Gave example test strategies and outputs.	4	8

Plans for the upcoming week

- ➢ Tyler Archer: I plan to obtain information about the UMC 65nm design rules and process features to determine how much changing is guaranteed to have to be done to our design to move it to this process, and determine if it's possible to scale our design down to 65nm in Cadence.
- ➢ Mahmoud Gshash: Look at the work needed to be done to modify the design to the new rules.
- ➢ Caroline Alva: I plan to continue creating a well defined test plan to determine the gain error and the offset error of the ADC. Once it is determined whether scaling is possible or not, I plan to help in anyway to move our design to the 65nm process
- ➢ Josh Rolles: Further research grouping test codes into one code for linearity and DNL tests. Assist in any 65 nm scaling if the scaling is possible.
- ➢ Caleb Davidson: Fix initial test plan thoughts based on feedback from team members. Try to formalize the definitions into an organized step-by-step process with exit criteria.