EE/CprE/SE 492 BI-WEEKLY REPORT 1 8/23 – 9/10

Group number: sddec18-20

Project title: Delta Sigma ADC

Client &/Advisor: Randall Geiger and Degang Chen

Team Members/Role:

Tyler Archer — Test Lead Engineer

Caleb Davidson — Communications and Scribe Manager

Caroline Alva — Chief Engineer

Mahmoud Gshash — Meeting Facilitator

Joshua Rolles — Report Manager

Weekly Summary

This week the team has been working on issues regarding the fabrication of the Delta Sigma ADC. This week we were informed that the PDK we are currently working on is a generic form of the 180nm PDK, we investigated whether this will cause us issues with the performance of the ADC or not. After discussing with multiple professors it was decided that fabrication in the generic PDK, would result in a satisfactory performance of the ADC. We have also realized that not all of the necessary tests were simulated before fabrication. The team has reached out to multiple people to ensure all necessary tests (metal fill, antenna rules) are completed before fabrication. The team also has started to investigate the tests that need to be completed after the fabrication of the ADC to characterize it.

Past week accomplishments

- **Tyler Archer:** Uses the MOSIS website to research the fabrication process for our process and the necessary design rule checks that must be done on our design. Met with Professors and ETG support to discuss the suitability of our technology library for creating a design that can be fabricated, design rule checks, creating GDSII files from our design, and other issues that may need to be addressed for preparing our design for fabrication. Corresponded by email with one of the co-creators of our technology library at NCSU to determine the sizing basis of the design rules and whether the resolution and grid spacing of our design is correct. Corresponded by email with a graduate student familiar with the fabrication process to attempt to identify resources for design rule checks/fixes for antenna rules and CMP density rules.
- **Mahmoud Gshash:** Spoke to Dr. Neihart and Steve from ETG, and Robert Buckly about the problems we had during extracting GDS II files for the 180 nm process. Robert provided us with a contact at NCSU to ask him about the process files.
- **Caroline Alva:** This week I have met with Dr. Geiger to ensure that the generic PDK would be functionally sufficient to fabricate the ADC in. I have attained the DRC and LVS scripts from Cadence to check if metal fill and antenna rules was a predetermined check included in either the DRC or LVS. I have began looking into the datasheets of other ADC to see what tests should be run to characterize the ADC.
- **Josh Rolles:** Researched common Delta-Sigma data converter data sheets to develop a comprehensive testing plan for our part assuming we receive it before the end of the semester.
- **Caleb Davidson:** Look at current DE-ADCs and figure out what sort of characteristics would be appropriate to test, for our chip, upon manufacturing.

Pending issues

- ➢ Tyler Archer: Information about fabrication with our technology library and resources for performing certain design rule checks has been difficult to find.
- ➢ Mahmoud Gshash: We need to find whether the installed files are generic files, or they are the actual process file that the manufacture requires.
- ➢ Caroline Alva: No issues currently, waiting to hear from MOSIS to ensure all of the simulations that needed to be completed before fabrication are completed.
- ➢ Josh Rolles: Deciding which tests to perform on part to characterize it. Not receiving the part back from fabrication like we had planned on.
- ➢ Caleb Davidson: In the past couple of weeks we have been trying to get past an issue we had with the PDK in order to fabricate.

Individual contributions

Name	Individual Contributions	Hours Worked	Cumulative Hours Worked
Tyler Archer	• Used the MOSIS website to research the fabrication process for our process and the necessary design rule checks that must be done on our design. Met with Professors and ETG support to discuss the suitability of our technology library for creating a design that can be fabricated, design rule checks, creating GDSII files from our design, and other issues that may need to be addressed for preparing our design for fabrication.	4	4

	Corresponded by email with one of the co-creators of our technology library at NCSU to determine the sizing basis of the design rules and whether the resolution and grid spacing of our design is correct. Corresponded by email with a graduate student familiar with the fabrication process to attempt to identify resources for design rule checks/fixes for antenna rules and CMP density rules.		
Mahmoud Gshash	• Spoke to Dr. Neihart and Steve from ETG, and Robert Buckly about the problems we had during extracting GDS II files for the 180 nm process. Robert provided us with a contact at NCSU to ask him about the process files.	4	4

Caroline Alva	• Meeting with Dr. Geiger regarding tests to be completed and the generic PDK • Meeting with Robert to investigate what checks are being completed by DRC and LVS • Investigating Datasheets of comparable ADC to establish testing after fabrication	5	5
Josh Rolles	• Researched common Delta-Sigma data converter data sheets to develop a comprehensive testing plan for our part assuming we receive it before the end of the semester.	4	4
Caleb Davidson	• Look at current DE-ADCs and figure out what sort of characteristics would be appropriate to test, for our chip, upon manufacturing.	5	5

Plans for the upcoming week

- Tyler Archer: Identify and obtain software for performing antenna rule and CMP density rule checks and fixing any violations that are found. Run these checks and fix any violations. Verify that our device resolution and grid spacing for our layout files all conform with the requirements for fabrication. Determine the correct way to create a GDSII file from our layout design. Run a simulation to test power consumption of our design.
- Mahmoud Gshash: Follow up with Tyler and the NCSU contact person to install the correct files to generate GDS II files.
- Caroline Alva: Provide an outline of tests and how to perform tests that need to be completed after fabrication of the ADC. To also ensure that the layout of the ADC is suitable for fabrication.
- Josh Rolles: Develop final list of pre-fabrication simulations and post-fabrication tests to be run on the ADC. Begin running any pre-fabrication tests left to run such as Gate to power, floating node, etc.
- Caleb Davidson: Using the tests we can build a test plan. We need to first determine how we are going to test each characteristic.