High-Resolution ADC Using Delta-Sigma Architectures

DESIGN DOCUMENT

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I_d: Diode Current
I_{ss}: Diode Reverse Saturation Current
$V_{d:}$ Voltage Across a Diode
V_t: Thermal Voltage
K: Boltzmann's Constant
T: Temperature

q: **Electron Charge**
n: **Number of Diodes**

1.5 List of Definitions

Integrated circuit (IC) – an electronic circuit formed on a piece of semiconducting material.

Analog to digital converter (ADC) – an electronic device that converts an analog signal to a digital signal without altering its essential content.

Throttle – control the operation speed of a circuit, and therefore its heat dissipation rate.

Sample – reduce a continuous-time signal to a discrete-time signal by collecting a series of its values at regularly spaced intervals.

Resolution – the number of discrete output values an ADC can produce over the range of analog input values.

Delta-Sigma ADC – an ADC that produces a high-resolution output signal using oversampling techniques.[1]

DAC – an electronic device that converts a digital signal to an analog signal without altering its essential content.

Modulator – an electronic device that varies one or more properties of a periodic waveform.

Digital Filter – a system that performs mathematical operations on a discrete-time signal to modify certain aspects of that signal.

Digital Decimator – a device that reduces the sampling rate of a digital signal.

Parasitic Capacitance – a usually unwanted capacitance that exists between parts of electronic components or circuits because of their proximity to each other.

Switched Capacitor Integrator – an electronic device that performs an integrating function using an operational amplifier and a switch-connected capacitor that acts as a current-limiting component.

Comparator – an electronic circuit that compares two voltages and outputs a digital signal indicating which voltage is larger.

Layout – a representation of an integrated circuit using geometric shapes that correspond to the patterns of the materials that makes up the physical integrated circuit.

2 Introductory Material

2.1 Acknowledgement

The development of this design is supported by faculty advisor Dr. Randall Geiger. We would like to thank Dr. Geiger for providing the key insight and expertise that greatly assists our project. His contributions are crucial in ensuring that our team fully comprehends the necessary technical material for this project.

2.2 Problem Statement

We rely heavily on various integrated circuits (IC) to perform as intended every day. Without these circuits, we would have a difficult time with typical day-to-day tasks. Heat can become a serious issue with ICs. When these chips overheat, it can damage the circuit and cause it to malfunction. There is a need for a method to measure and communicate the chip temperature to circuitry that will throttle the circuit activity when necessary.

Our team has proposed to design a temperature sensor and a Delta-Sigma Analog-to-Digital Converter (ADC) to convert the temperature sensor's output to a digital signal. This circuit will accurately measure, and communicate in a digital format, the temperature of the IC. With this technology, the temperature of an IC can be monitored and controlled as it is being used to ensure that it doesn't overheat.

2.3 Operating Environment

Our circuit can be integrated with any IC as it is intended to monitor the temperature of that IC. The operating environment will vary depending on the system the circuit is integrated with. For most purposes, this will result in the circuit being used in a small-enclosed environment.

2.4 Intended Users and Intended Uses

Our product is to be used by IC designers when designing new ICs. They will integrate our circuit with the IC they are designing. IC designers in both industry and in academic research will use this ADC circuit. Our product will be used to measure and communicate the temperature of an IC to other parts of the IC responsible for temperature control. Based on the output of our circuit, the connected circuitry will change the IC's rate of activity to reduce heat dissipation when the temperature rises above a certain threshold

2.5 Assumptions and Limitations

Assumptions:

- The temperature of the IC in which the temperature sensor and ADC are used will remain between 10 degrees and 60 degrees Celsius.
- Two accurate reference voltages of 765 millivolts (Vref) and 800 millivolts (Vref+) will be provided to the ADC for the original 180nm design.
- Two accurate reference voltages of -200 millivolts (Vref) and 200 millivolts (Vref+) will be provided to the ADC for the 65nm design.

Limitations:

- The area of the physical layout for the 180nm circuit is no more than 4 millimeters by 4 millimeters.
- The area of the physical layout for the 65nm circuit is no more than 0.5 millimeters by 1 millimeter.
- The 65nm design is limited to 20 I/O pins
- The supply voltages are V_{SS} = 0V V_{DD} =1.8V for the 180nm design.
- The supply voltages are V_{SS} = -1.25V V_{DD} =1.25V for the 65nm design

2.6 Expected End Product and Other Deliverables

The end product will be an IC design containing an ADC. It will be submitted for fabrication by the end of the fall 2018 semester. The fabricated IC will be received in time to test it during the spring 2019 semester. A testing plan described in section 4 has been created and a PCB will be sent for fabrication. The PCB will be used for testing the IC. A DAQ will gather data from the ADC and from the data several spectral characteristics can be extracted. Depending on the test results, changes may be made to the ADC and a revised version will be sent again for fabrication. The end goal is to have this ADC suitable to be implemented in graduate research projects.

3 Specifications and Analysis

3.1 Specifications

The original specifications that this project is designed to meet are the following:

- The circuit should be designed in the 0.18 um TSMC CMOS process.
- The area of the physical layout is to be no more than 4 millimeters by 4 millimeters.
- The ADC should output at least 1 output code per 10 milliseconds.
- The ADC should have a targeted resolution of 10 bits.
- The temperature sensor should have a monotonic relationship between temperature and output voltage.
- The temperature sensor and ADC system should be able to measure temperatures in the 10-degree to 60-degree Celsius range.

The new specifications that this project is designed to meet are the following:

- The circuit should be designed in the 65 nm UMC CMOS process.
- The area of the physical layout is to be no more than 0.5 millimeters by 1 millimeter.
- The ADC should output at least 1 output code per 10 milliseconds.
- The ADC should have a binary stream output.
- The ADC should include no more than 20 I/Os

3.2 Approach

There are a large variety of data converter architectures that are currently available. This project specifically asked for the design of a Delta-Sigma Data Converter although other designs considered were a SAR and Nyquist rate data converter. The SAR (Successive-approximation) data converter is one of the oldest and most common data converter architectures. The SAR is used when there are multiple inputs, and it is mainly implemented in industrial control applications. The Nyquist data converters are data converters sampled at the Nyquist rate frequency. These data converters cannot reach a high resolution and experience a higher level of quantization noise at the output.

The chosen design, the Delta Sigma ADC, has characteristics that make it the best fit for our application of measuring the voltage output of a temperature sensor. The delta-sigma ADC experiences a low level of quantization noise at the output. This is achieved through oversampling of the input signal. The Delta Sigma architecture produces a high-resolution output, which will provide an accurate temperature reading from our sensor. Our delta-sigma ADC design is based on the design in the textbook *Analog Integrated Circuit Design*[4]. We modified the design to use first-order modulator and decimator circuits instead of higher-order circuits. The strengths of the first-order circuit are that it is sufficient for providing the desired output, makes the circuit easier to design and build in the short time we have, and allows for a circuit with a very small die footprint. A weakness in choosing this simpler design is that the first-order circuit will not carry out noise shaping in the ADC which would result in a more accurate output and is exemplified in the *IEEE Journal of Solid-State Circuits* article, "A 43-mW MASH 2-2 CT ΣΔ Modulator Attaining 74.4/75.8/76.8 dB of SNDR/SNR/DR and 50 MHz of BW in 40-nm CMOS."[6]

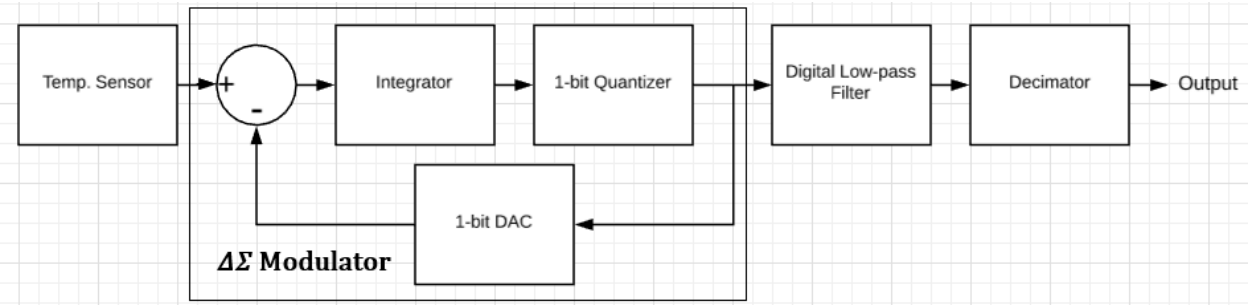


Figure 3.2.1: Delta-Sigma ADC Block Diagram

Our approach for this project is to implement an integrated circuit consisting of a temperature sensor and delta-sigma ADC using the top-level architecture shown in Figure 3.1. The design consists of a temperature sensor, a delta-sigma modulator, and a digital filter/decimator. The ADC is designed to take samples of the temperature sensor output at a rate of 102.4 kHz and output a 10-bit binary representation of the temperature at a data rate of 100 Hz.

3.3 Temperature Sensor

Temperature is a physical quantity that can be identified as a low frequency analog signal. For example, the temperature in a room will not change a few degrees in a matter of one or two milliseconds. To measure temperature the sensor needed to be designed using a temperature dependent device. The design used in this project implemented diodes as the temperature dependent devices. The equation for the current through a diode is given in as[4]:

$$\mathbf{Id} = \mathbf{Iss} * (e^{Vd/Vt} - 1) \quad (3.3.1)$$

Fixing the current across the diode allows the voltage across the diode to change as the thermal voltage changes. The design of the temperature sensor is shown below, this circuit produces a linear and accurate output.[5]

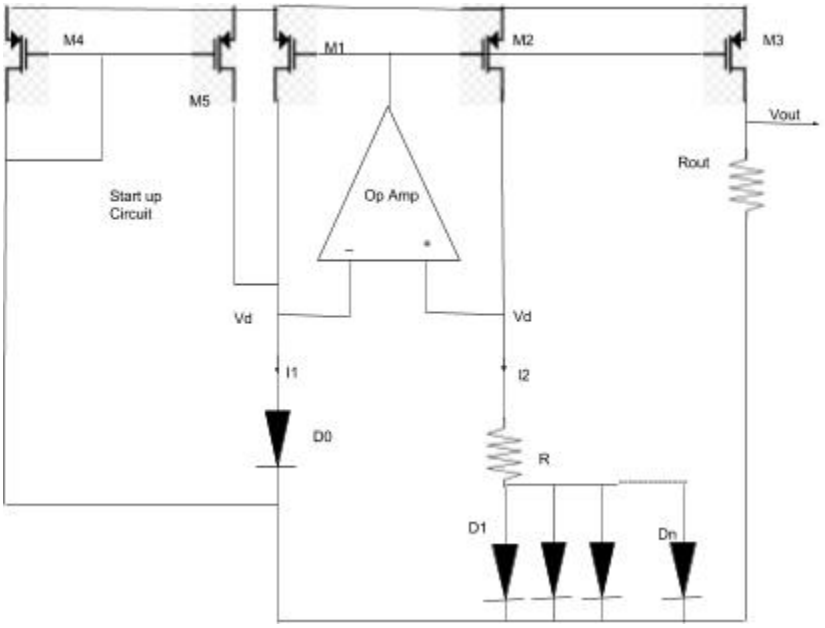


Figure 3.3.1: Temperature Sensor Structure

The output of the circuit is given by the following equation:

$$\mathbf{V_{out}} = \frac{KT}{q} * \frac{R_{out}}{R} * \ln(n) \quad (3.3.2)$$

A diode can simply be implemented using a diode-connected transistor, where the gate of the transistor is connected to its drain. The operational amplifier used in this design is a single-stage telescopic cascode operational amplifier.

A Cadence schematic of our temperature sensor design is shown in Figure 3.3.2. It includes a unity-gain buffer using an op amp to buffer the output. This prevents loading of the output of the temperature sensor from affecting the voltage produced at the output.

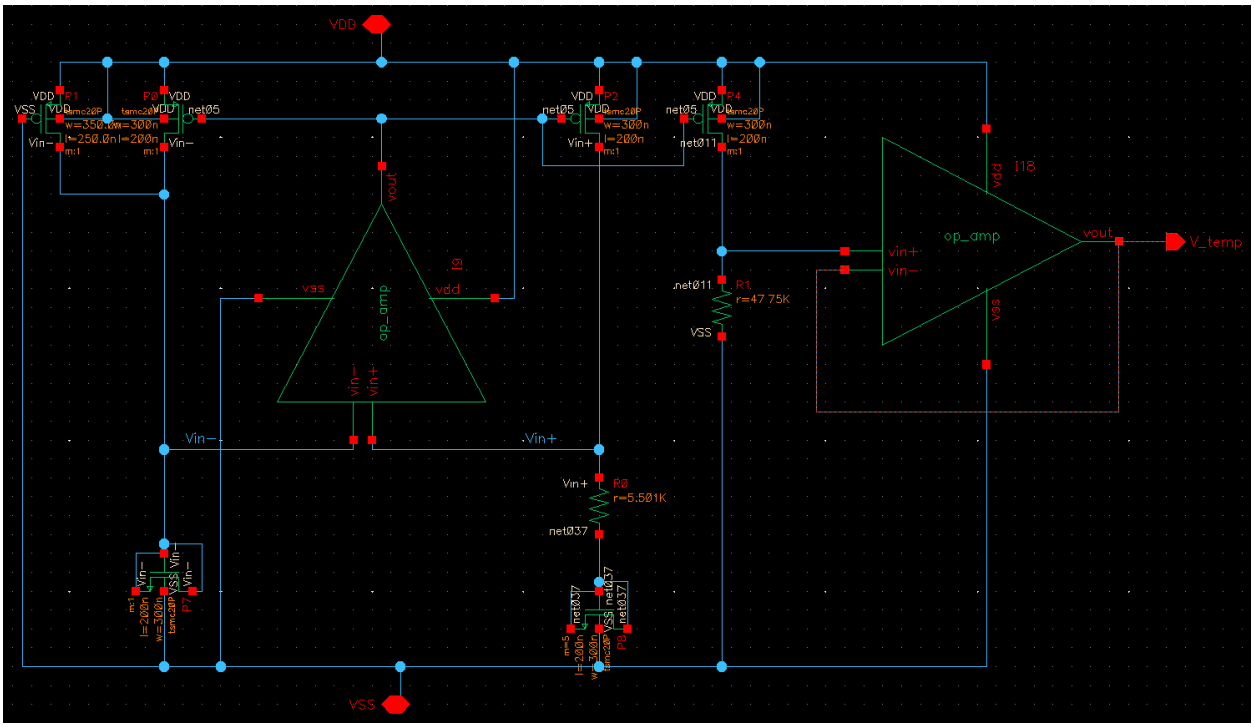


Figure 3.3.2: Temperature Sensor Schematic

3.4 Clock

A ring oscillator, which consists of a ring of 23 inverters, generates the main clock, which has a frequency of 1638.4 kHz. This is converted to clk1, clk2, clk3, and clk4 signals using a 4-bit counter and a combinational logic circuit. The frequency of the resulting four clock signals is 102.4 kHz. The signals have various duty cycles and phases to time the operation of different parts of the ADC relative to one another. The clock circuit diagram is shown in Figure 3.4.1.

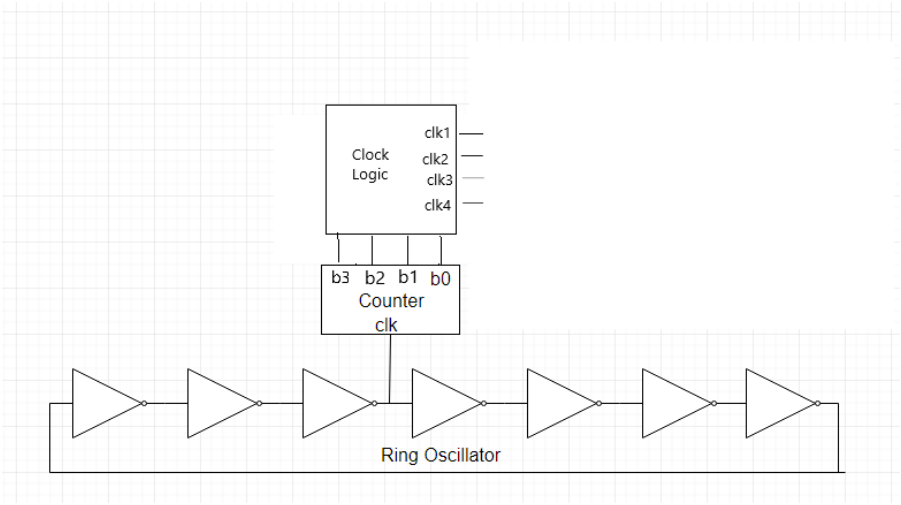


Figure 3.4.1: Clock Generating Circuit Diagram

Figure 3.4.2 shows the Cadence schematic of the clock circuit.

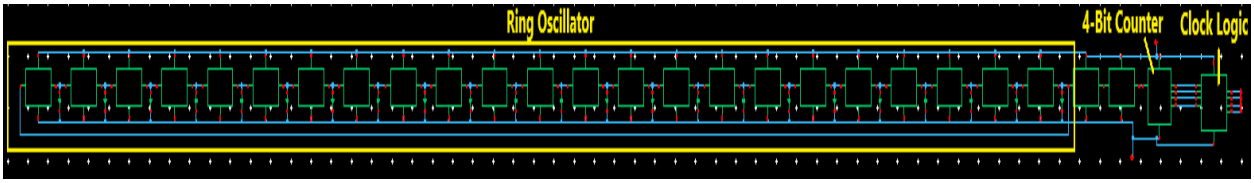


Figure 3,4.2: Clock Generating Circuit Schematic

Figure 3.4.3 shows the Cadence schematic of the clock logic. The Reg_DFF blocks are flip-flops used to latch the clock outputs to avoid unwanted spikes during high and low times.

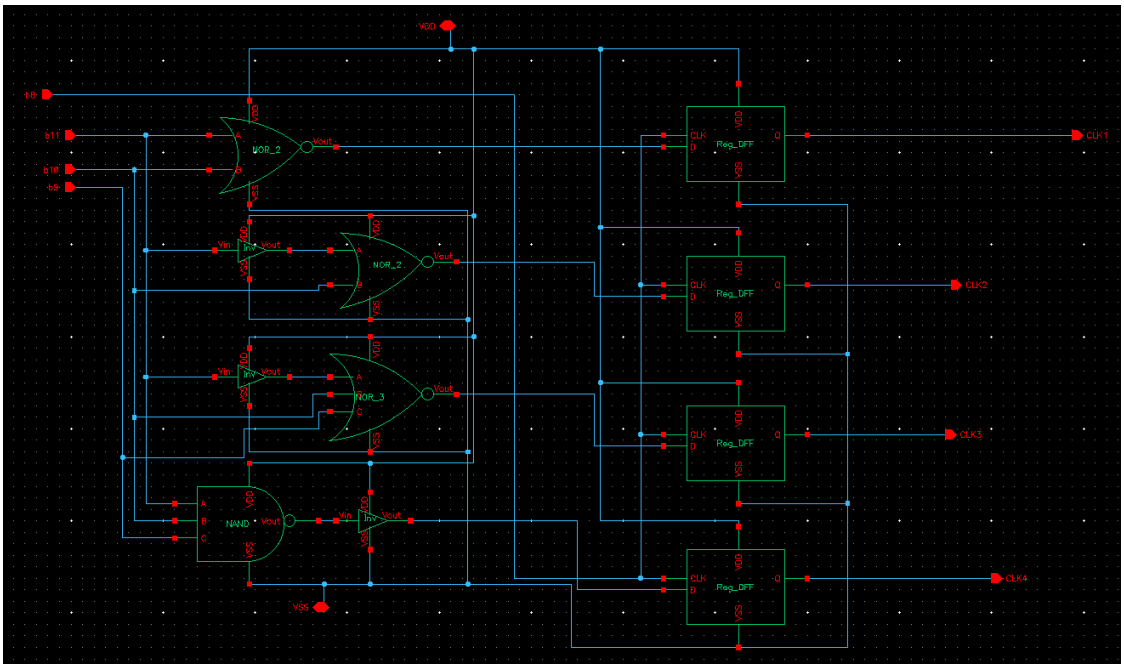


Figure 3,4.3: Clock Logic Schematic

The four resulting clock signals and their purposes are shown in Figure 3.4.4.

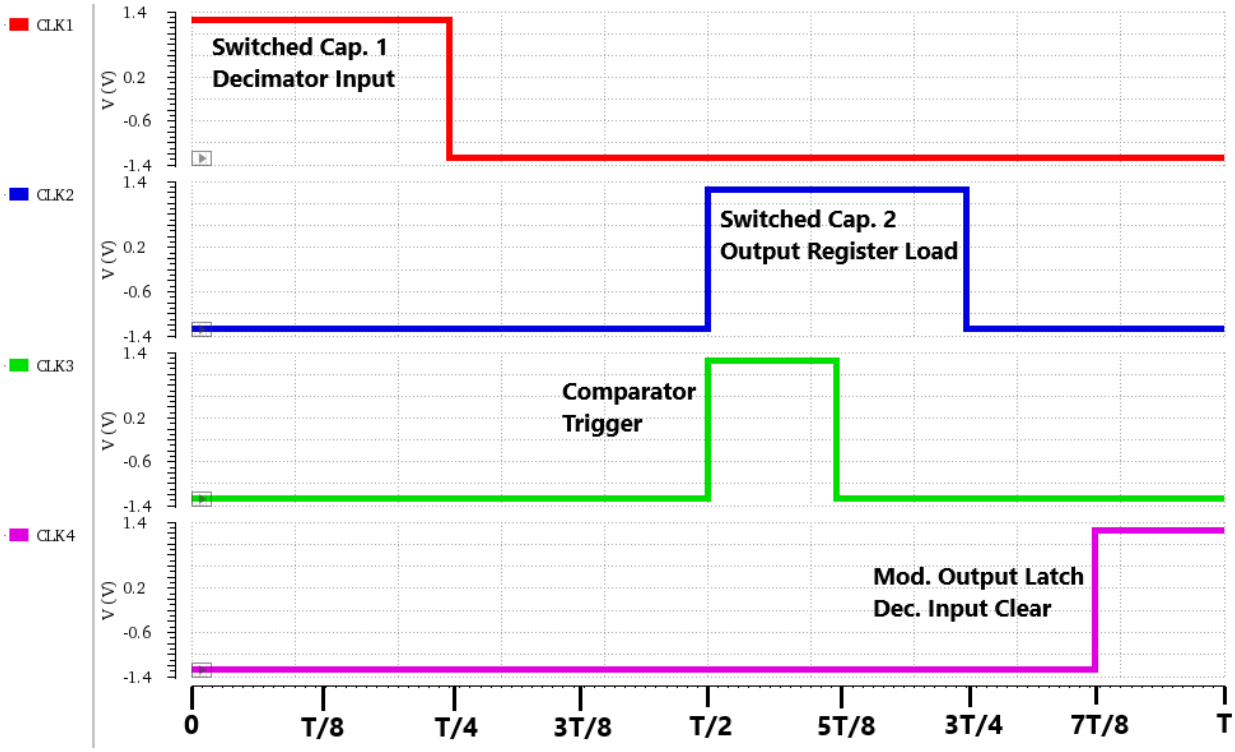


Figure 3,4.4: Clock Signal Timing Diagram

3.5 Delta-Sigma Modulator

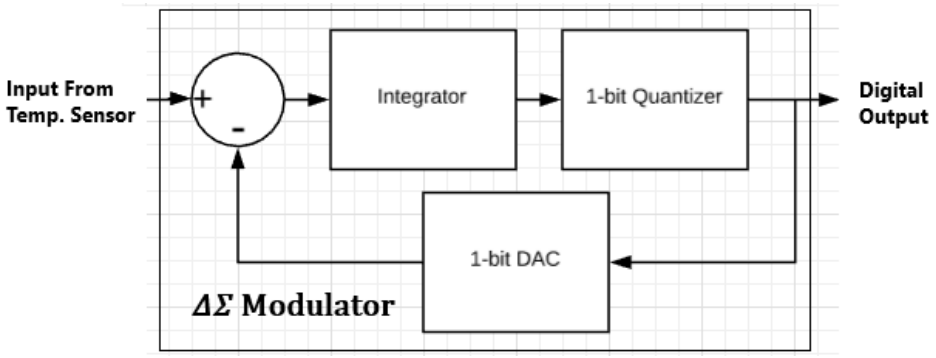


Figure 3.5.1: Block Diagram of Delta-Sigma Modulator

The delta-sigma modulator is the first of the two main parts of the delta-sigma ADC. The modulator takes the analog output of the temperature sensor as its input, and outputs a digital signal that contains the

temperature data in the form of a data stream whose proportion of 1's to total values in a 10-millisecond time span is equal to the magnitude of the input voltage to the modulator relative to the input voltage range. The modulator contains three main functional blocks: an integrator, a 1-bit quantizer (a comparator), and a 1-bit DAC. The Cadence schematic of our modulator is shown in Figure 3.5.2.

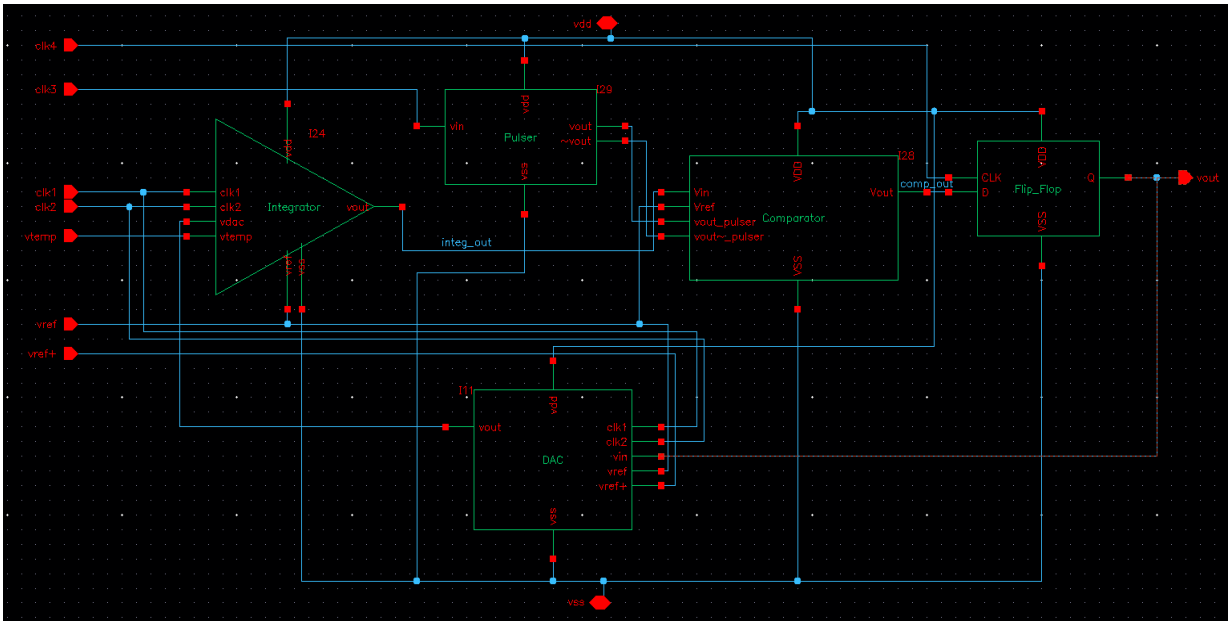


Figure 3.5.2: Schematic of Delta-Sigma Modulator

3.5.1 INTEGRATOR

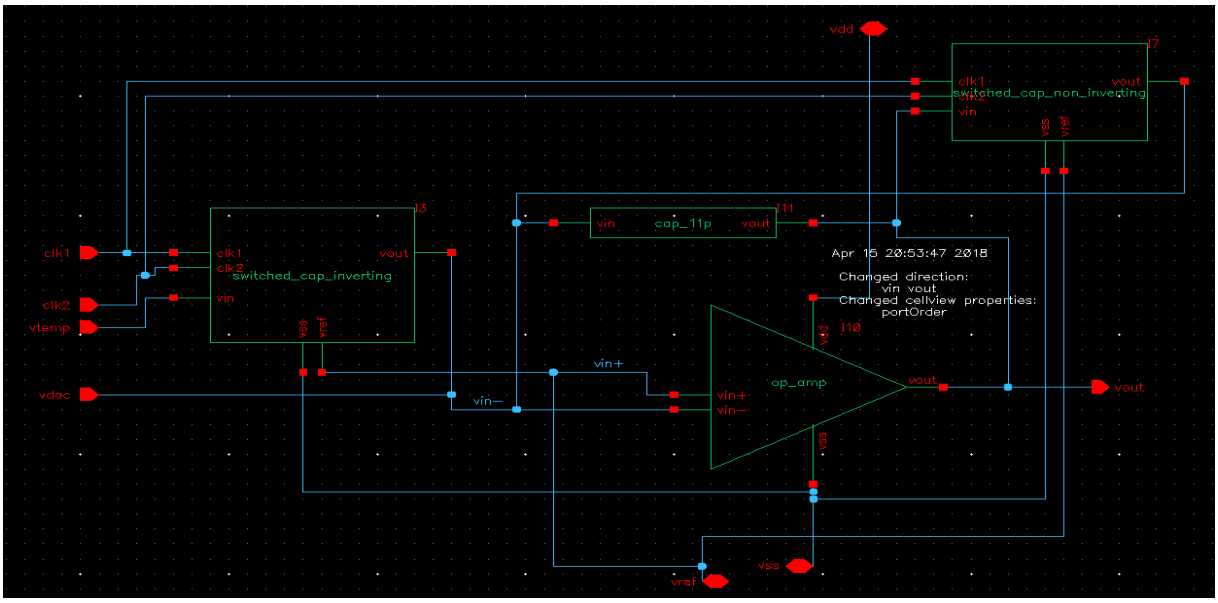


Figure 3.5.1.1: Integrator Schematic

The integrator is the functional block that generates a sawtooth wave that acts as the input to the comparator. The voltage output of the integrator progresses in a negative or positive direction depending on the sign of the input voltage.[1] The slope of this progression depends on the magnitude of the input voltage. The integrator consists of an op amp with a feedback capacitor, a feedback switched-capacitor, and a switched-capacitor input. The input switched capacitor input acts as a resistance for the ADC input. The feedback capacitor performs the integrating function by accumulating charge. The feedback switched capacitor acts as a resistor that prevents error from accumulating on the output due to charge accumulating on the feedback capacitor from offset voltage.

The output of the integrator is a saw-tooth wave. The proportion of the time that this wave is above the comparator's switching voltage (768.5mV) is proportional to the magnitude of the input voltage to the ADC relative to the input voltage range (730mV to 800mV). The integrator outputs with a range of input voltages applied are shown in Figure 3.5.1.2. Input voltages are expressed as a percentage of the input voltage range at the left side of the figure. The black lines are the comparator's trip voltage.

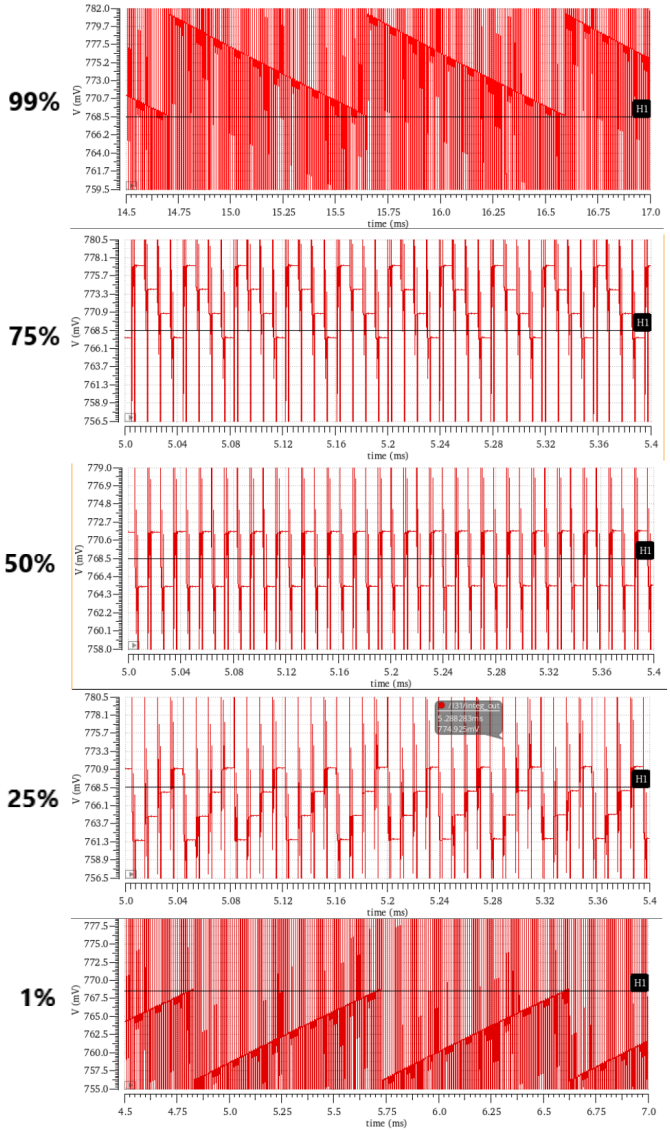


Figure 3.5.1.2: Integrator Outputs with Various Input Voltages Applied

3.5.2 SWITCHED CAPACITOR

The switched capacitor circuits each consist of a capacitor and four switches. The circuit can be made to be either inverting or non-inverting by simply changing the clocking of the switches. Clock 1 and Clock 2 are 180-degrees out of phase and have 25% percent duty cycles to ensure that they do not overlap, preventing a short-circuit from Vin to ground (or to Vref in the case of our circuit). Diagrams of each type of switched capacitor circuit are given in Figures 3.5.2.1 and 3.5.2.2.

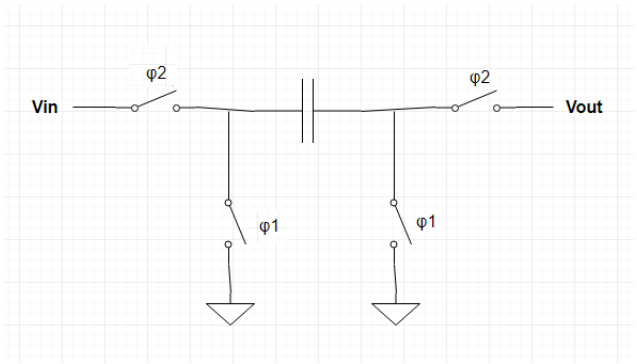


Figure 3.5.2.1: Non-Inverting Switched Capacitor Circuit Diagram

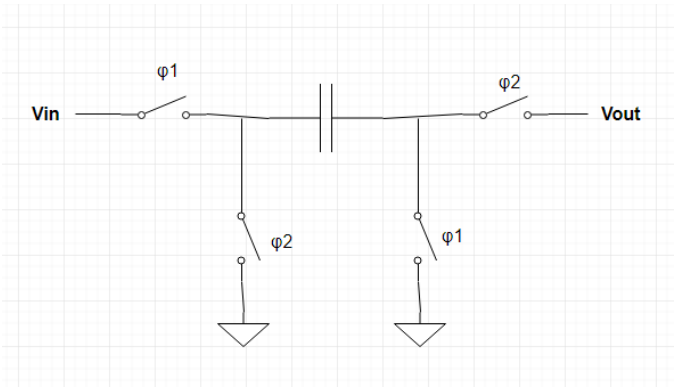


Figure 3.5.2.2: Inverting Switched Capacitor Circuit Diagram

The switched capacitor circuits act as resistors by restricting the flow of charge through them. The effective resistance is given by:

$$R_{EFF} = \frac{1}{C * f_{CLOCK}}. \tag{3.5.2}$$

Using a switched capacitor circuit allows a large resistance to be provided without the large die space consumption of a resistor.

We implemented the switches using NMOS devices (Figure 3.5.2.3).

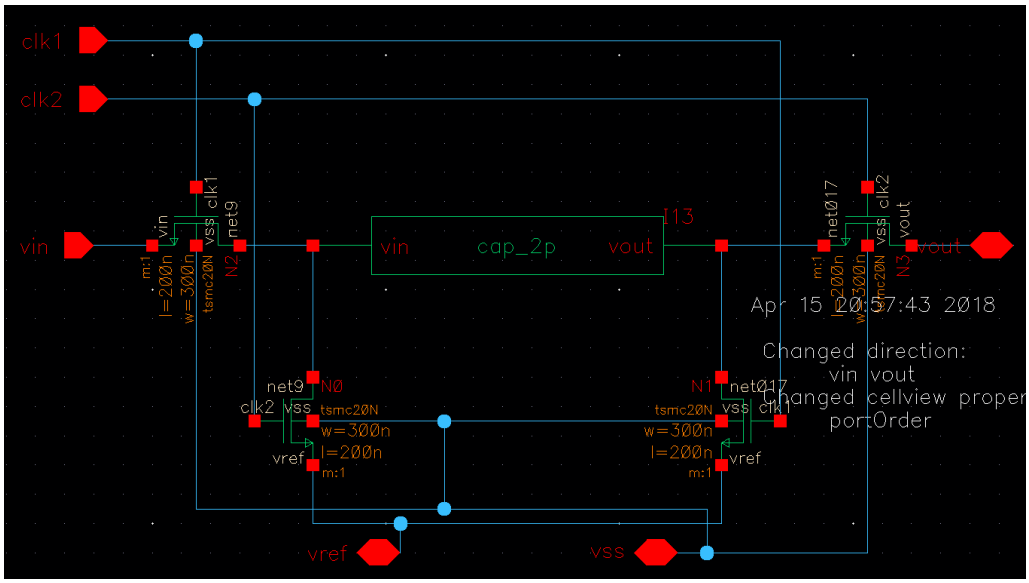


Figure 3.5.2.3: Inverting Switched Capacitor Circuit Schematic

3.5.3 Operational Amplifier

The operational amplifier used in our integrator has a single-stage telescopic cascode architecture (Figure 3.5.3.1)

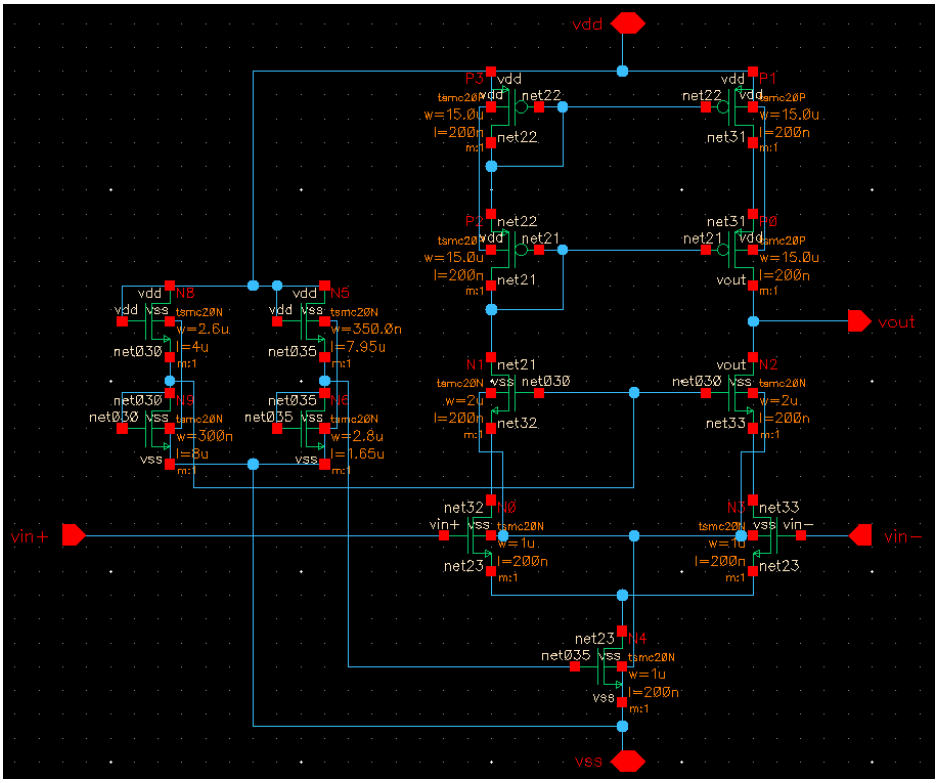


Figure 3.5.3.1: Telescopic Cascode Op Amp Schematic

Using the architecture in Figure 3.5.3.1 allows for a high gain (~70dB) without the necessity of adding on a second stage. This avoids the need for a feedback capacitor, which would take up a large amount of die space.

3.5.4 COMPARATOR

A 1-bit ADC reads in a voltage and produces a 1-bit digital output, such as 1 or 0. A comparator reads in a voltage and compares it to a voltage reference and outputs VDD or VSS, which are interpreted as a 1 or 0. A dynamic comparator only produces an output at a clock edge. The dynamic comparator uses strong positive feedback for a regeneration phase when a clock is high and passes through a reset phase when the clock is low. Using a clocked dynamic comparator allows us to sample the output of the integrator only at a point in the clock cycle when it is stable. This allows the comparator's output to be unaffected by the large spike in the integrator output seen in Figure 3.5.1.2.

The dynamic comparator that was used in the Delta Sigma data converter is shown in Figure 3.5.4.1.

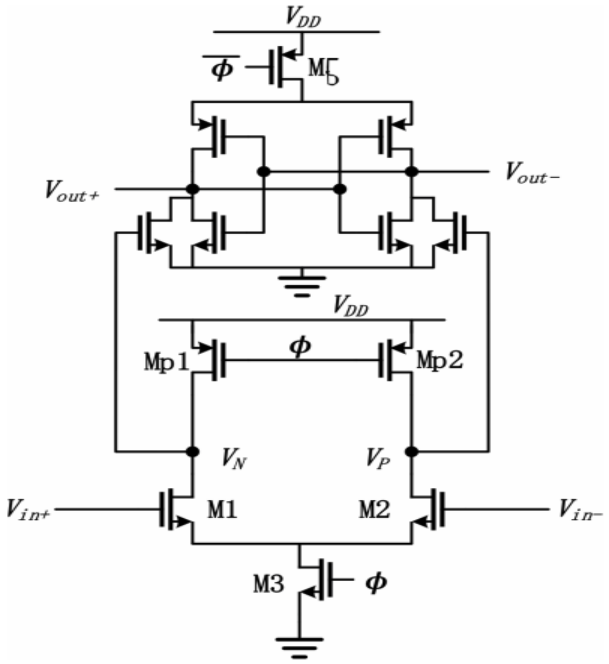


Figure 3.5.4.1: Dynamic Comparator Diagram

Functionality of the Dynamic comparator:
The dynamic comparator shown above is a conventional double tail comparator with a preamplifier[1]. This dynamic comparator will amplify a small voltage signal difference between V_{in} and V_{in-} allowing the latch to function accurately. When the clock ϕ goes low both the PMOS and NMOS tail transistors turn off and the nodes V_N and V_P have voltages at VDD. The tail transistors turning off also will avoid static power dissipation. When the clock ϕ goes high the voltages at the output will be discharged by the bottom transistors M1, M2, and M3. The nodes V_N and V_P will begin to drop and different rates due to the input voltages and transistors M1 and M2. If M1 has a larger input voltage than M2 the voltage at V_N will drop faster than the voltage at V_P. This will cause a smaller gate to source voltage on transistor M4 than M5, and a smaller current at V_{out+} than V_{out-}. The regenerative latch acts like an SR latch and pulls one output high and one low. Essentially if V_{in} is larger than V_{ref} it pulls V_{out} to VDD and V_{out-} to VSS, if V_{in} is smaller than

V_{ref} it pulls V_{out} to VSS and V_{out-} to VDD, if V_{in} is equal to V_{ref} it will enter a metastable state and produce one of the previously stated outputs.[6]

Shown below is the timing diagram of ϕ and $\bar{\phi}$ and the voltages at nodes V_N and $V_{P;\,it}$ is shown that when ϕ is low V_N and V_P are at VDD and they begin to discharge when ϕ is high.

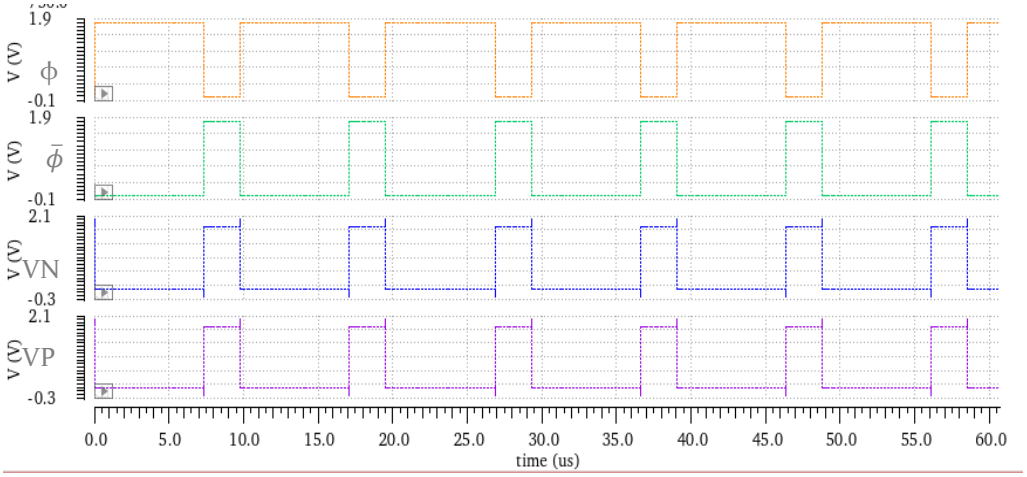


Figure 3.5.4.2: Comparator Clocking

Shown below is the timing diagram of ϕ, $\bar{\phi}$, $V_{in,}$ $V_{ref,}$ and $V_{out.}$ It is shown that the output will not compare the input voltage and the reference voltage until it is at a clock edge. The first line shows where V_{in} surpasses V_{ref} and the second line shows where the clock edge occurs, and V_{out} goes high.

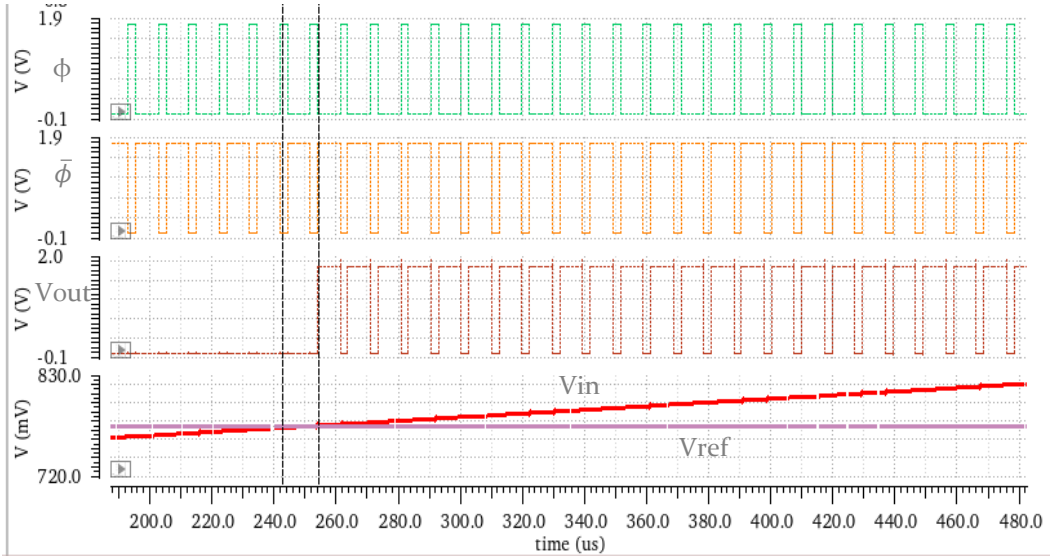


Figure 3.5.4.3: Dynamic Comparator Timing Diagram

The output of the comparator acts as the output of the delta-sigma modulator. The comparator's output is latched with a flip-flop (Figure3.5.2) to maintain consistent input to the DAC during each complete clock cycle. The comparator's output is shown for several modulator input voltages in the input voltage range. Input voltages are expressed as a percentage of the input voltage range at the left side of the figure.

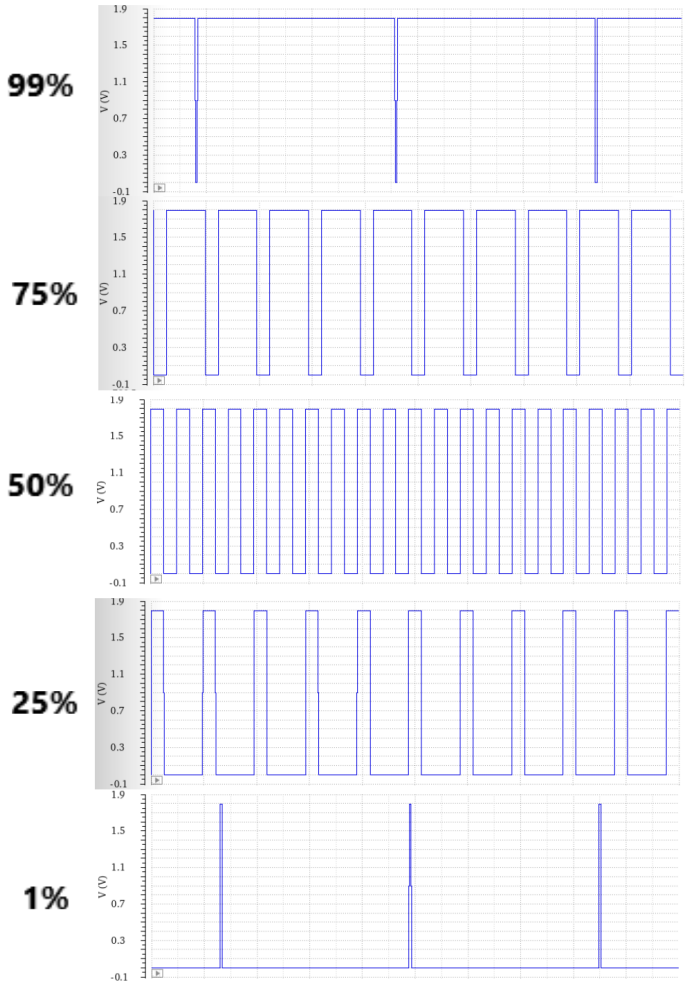


Figure 3.5.4.4: Comparator Outputs with a Range of Input Voltages Applied to ADC

The schematic of our comparator is shown in Figure 3.5.4.5

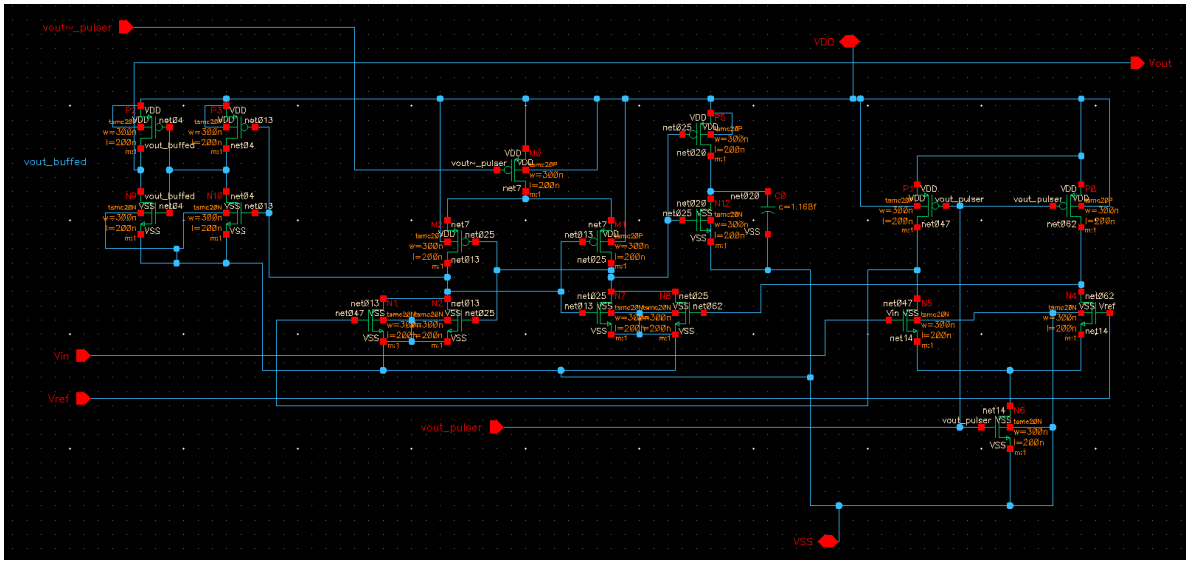


Figure 3.5.4.5: Comparator Schematic

3.5.5 Pulsing Circuit

When the dynamic comparator is in its armed state (ϕ low), its power dissipation is higher than when it is in its latched state. To minimize the power dissipation, we minimized the length of time the comparator is in its armed state during each clock cycle by pulsing ϕ low for only a very short time. We generated this pulse using a pulsing circuit. This pulsing circuit takes an input down-pulse of arbitrary length, and outputs a down-pulse of very short length (~3.9ns) on the falling edge of the input pulse. The schematic of the pulsing circuit is shown in Figure 3.5.5.1.

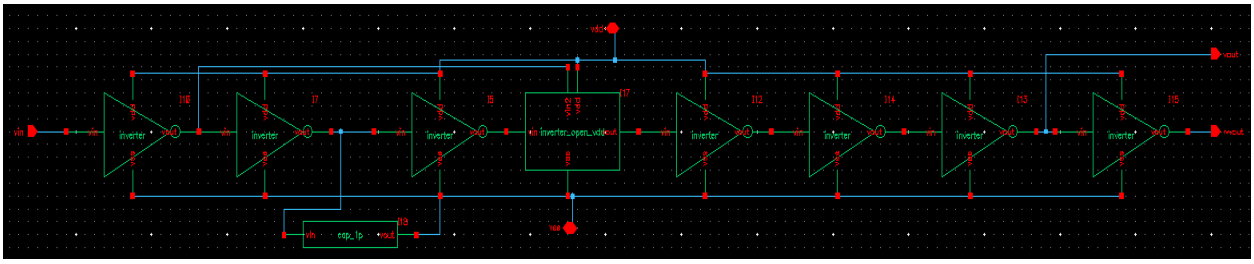


Figure 3.5.5.1: Pulsing Circuit Schematic

The pulsing circuit consists of seven inverters, one inverter with a switchable V_{DD} input (the rectangular component in the middle of the schematic), and a capacitor. When the clock's falling edge arrives at the input of the pulsing circuit, the output of the first inverter goes high, supplying V_{DD} to the switchable inverter. This causes the output of the switchable inverter to go high, making the output of the pulsing circuit (ϕ) go low. Once the clock signal propagates through the first three inverters and reaches the input of the switchable inverter, the output of the switchable inverter (ϕ) is made to go high again. The width of the pulse at the output is controlled by the size of the capacitor, which controls the propagation speed of

the input signal to the input of the switched inverter. A complementary output (ϕ-bar) is also generated with an extra inverter. The pulse generated at the output of the pulsing circuit is shown in Figure 3.5.5.2. The input clock signal is shown in blue. The output pulse is red.

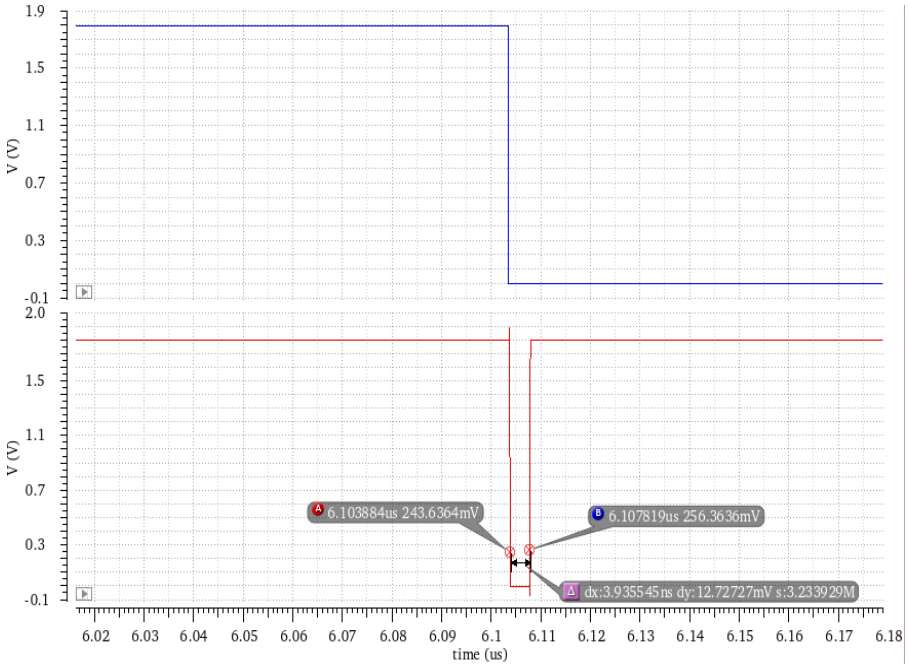


Figure 3.5.5.2: Pulsing Circuit Transfer Characteristic

3.5.6 DAC

The 1-bit digital-to-analog converter (DAC) functions to take a digital input from the output of the comparator and convert it into an analog signal to be applied to the input of the integrator. This is accomplished using a switched capacitor with V_{ref+} connected to the input. By using the output of the comparator to control the clocking of the switched capacitor via two multiplexers, a positive or negative current is applied at the DAC's output depending on the output level of the comparator. By configuring the control switching appropriately, the modulator diagram's differencing block (Figure 3.2.1) is also implemented by the DAC. The DAC's circuit configuration is shown in the schematic in Figure 3.5.6.1.

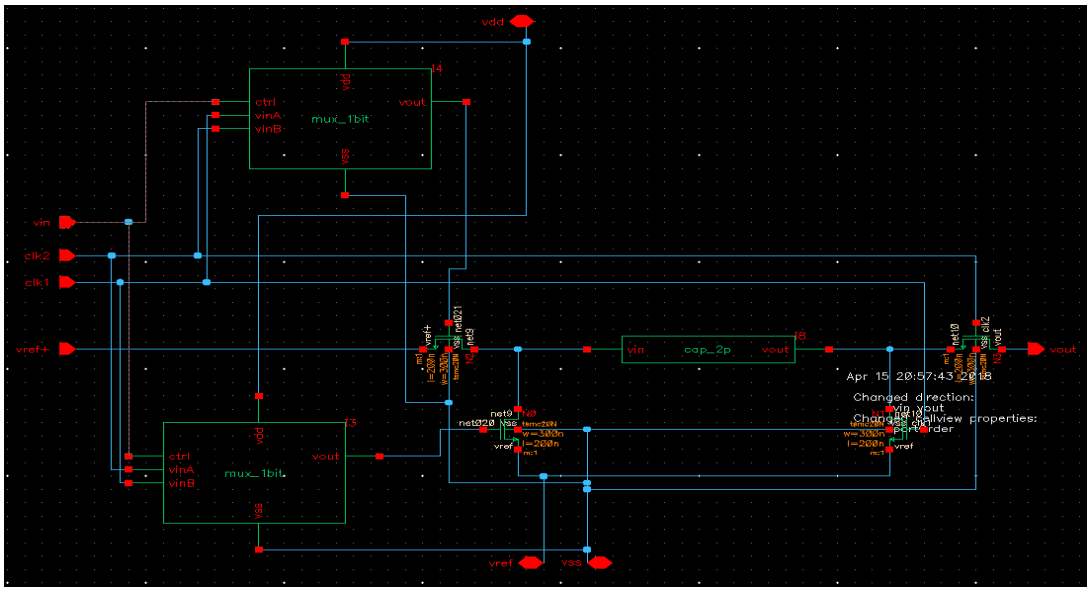


Figure 3.5.6.1: DAC Schematic

3.6 Digital Decimator

The digital portion of the delta-sigma ADC consists of a digital decimator. This block's function is to convert the binary data stream applied to its input by the modulator to a lower-frequency 10-bit parallel output. It accomplishes this by summing the inputs over 1024 clock cycle time spans and asserting these sums at its output. This results in a new output code every 10 milliseconds. The summing is accomplished by a 10-bit counter. The sum is then loaded to a 10-bit output register after every 1024 clock cycles, at which point the counter is reset. The loading of the register and resetting of the counter is controlled by another 10-bit counter, which acts as a clock divider of the 102.4 kHz system clock. The schematic of this circuit is shown in Figure 3.6.1.

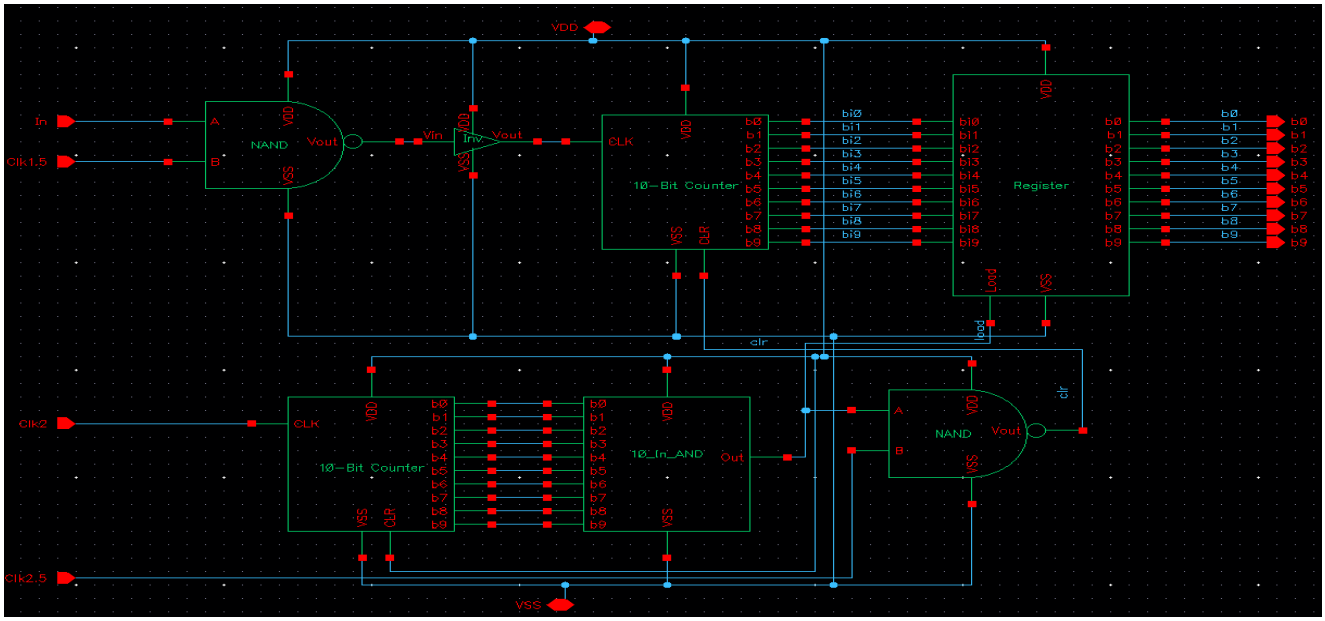


Figure 3.6.1: Decimator Schematic

The oversampling at the input of the modulator, followed by the 1024:1 decimation of the modulator's output signal, is what allows for the high accuracy of the delta-sigma ADC.

3.7 Physical Layout

Once we completed our circuit schematics, we used Cadence tools to create a physical layout of our circuit which is used to specify how the circuit will be fabricated. Most of the area of the layout is taken up by the three large capacitors in our integrator circuit. However, since these were built using the Metal 5 and Metal 6 layers, this left many layers below to build the rest of our circuit layout. The area of our complete layout is 174um x 240um, which is well within our maximum area constraint of 4mm x 4mm. The full circuit layout with capacitor visibility removed is shown in Figure 3.7.1.

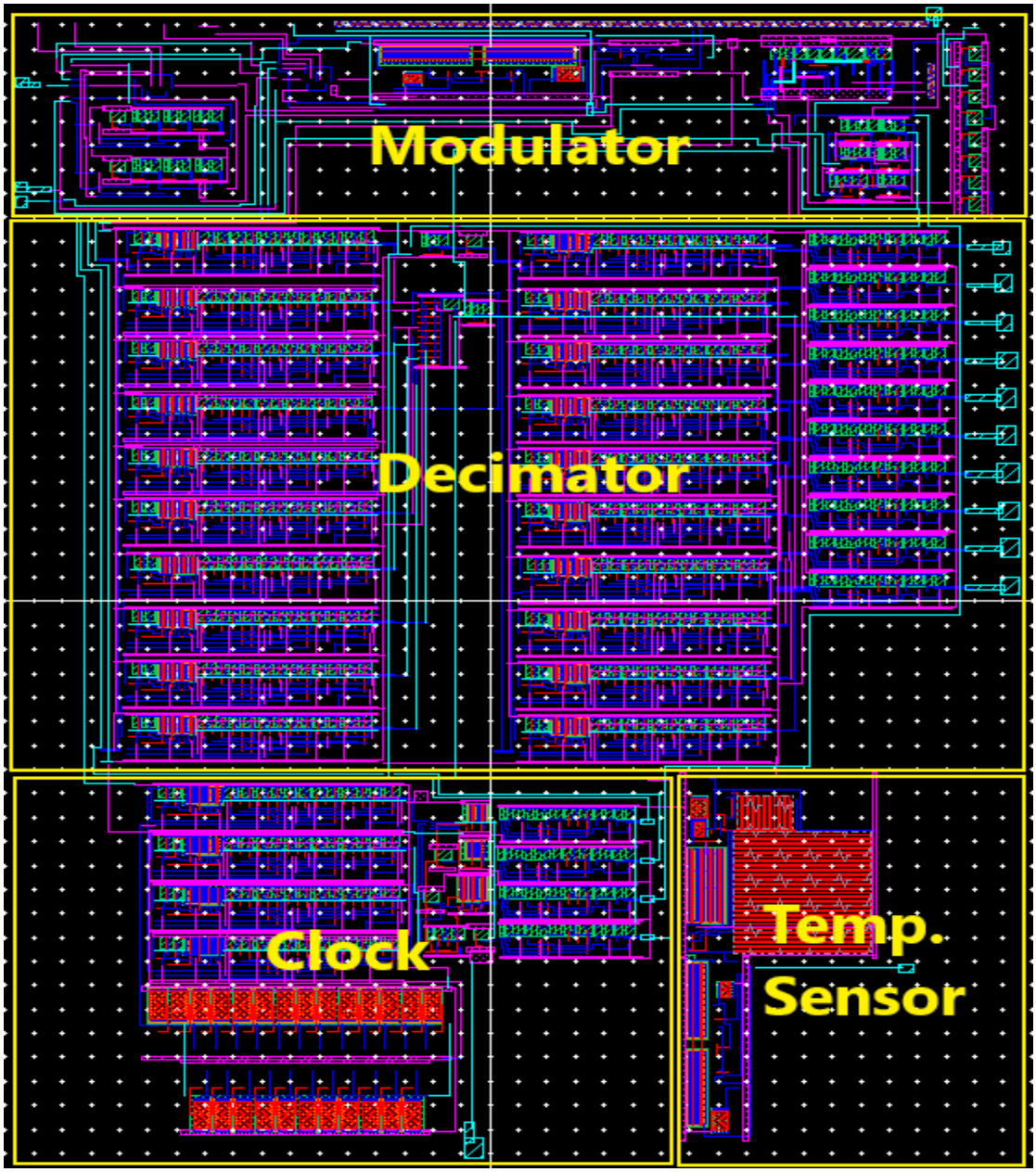


Figure 3.7.1: Complete Circuit Physical Layout

We used MIMS capacitors for the four large capacitors in our circuit because this type of capacitor has the highest capacitance per unit area (1fF/um^2). MIMS capacitors utilize the Metal 5, Metal 6, and Metalcap layers. The layout of the large capacitors is shown in Figure 3.7.2.

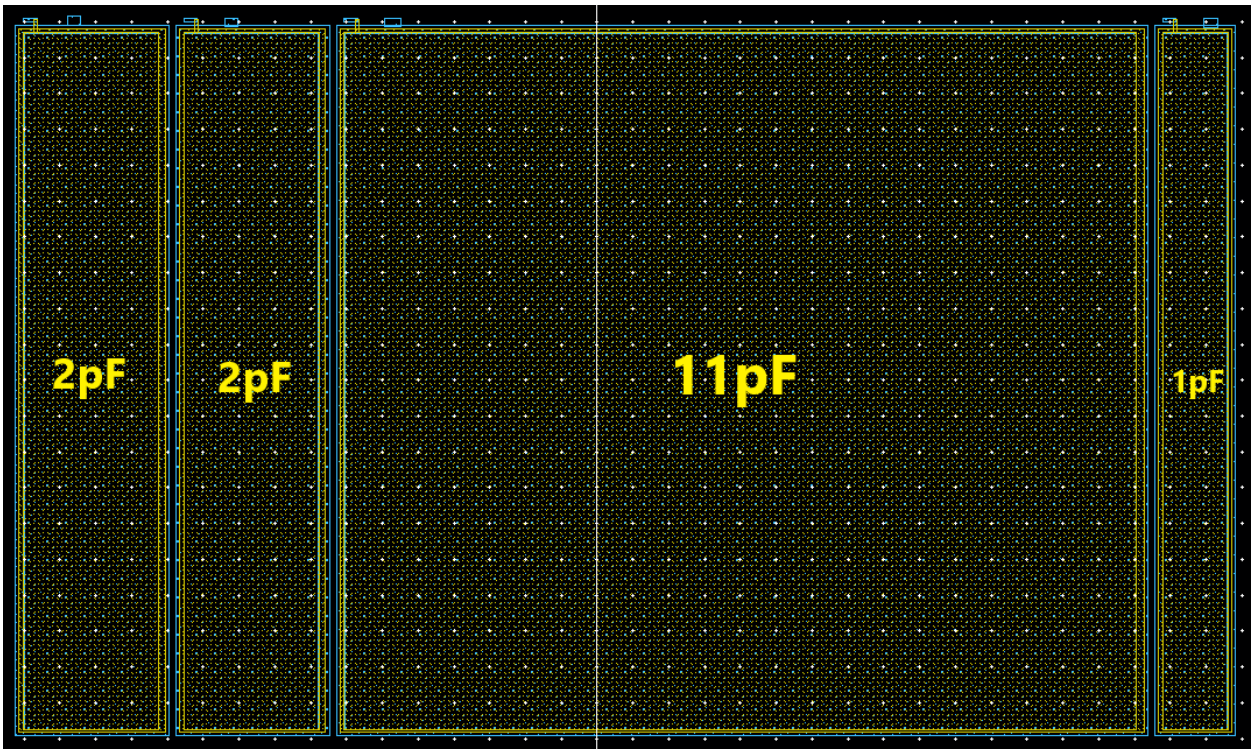


Figure 3.7.2: Layout of Large Capacitors

3.7.1 Modulator Layout

We constructed the layout for the modulator with the goal of keeping analog signal interconnects as short as possible to avoid introducing error into our analog signal due to parasitic resistances and capacitances. We placed the DAC and inverting switched capacitor circuit, where the input to the modulator comes in, near the input to the integrator op amp. We placed the input of the comparator near the output of the integrator op amp. We placed the noninverting switched capacitor circuit next to the op amp since it connects to both the op amp's input and output. We then placed the flip-flop and pulser in some of the remaining area on the right side of the layout. We used metal 1 for most of the connections within each component, metal 2 for most of the connections between components, and metal 3 for the longer connections between components. The higher metal layers have lower parasitics, so were used for longer interconnects to avoid signal degradation. The layout of the modulator is shown in Figure 3.7.1.1.

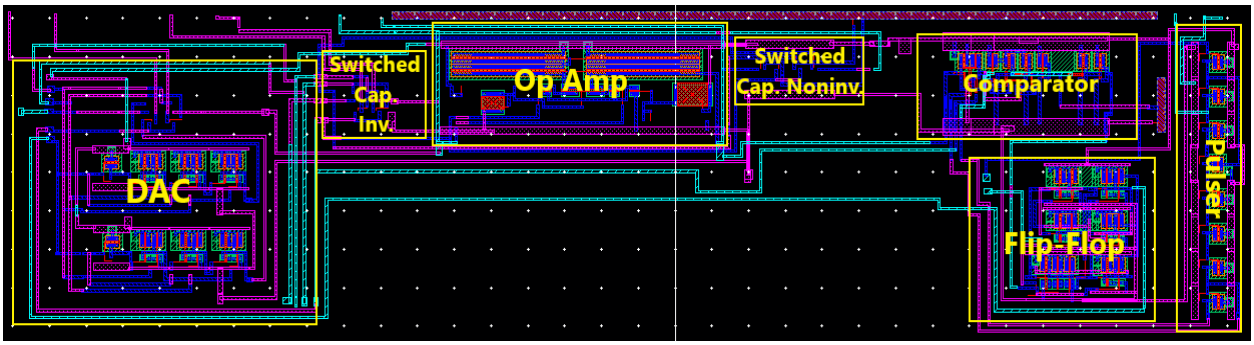


Figure 3.7.1.1: Modulator Layout

3.7.2 Decimator Layout

We constructed the layout for the decimator using the same goals as for the modulator, placing the inputs of component blocks near the outputs of the blocks feeding them to avoid signal degradation due to large parasitics in longer interconnects. The layout of the decimator is shown in Figure 3.7.2.1.

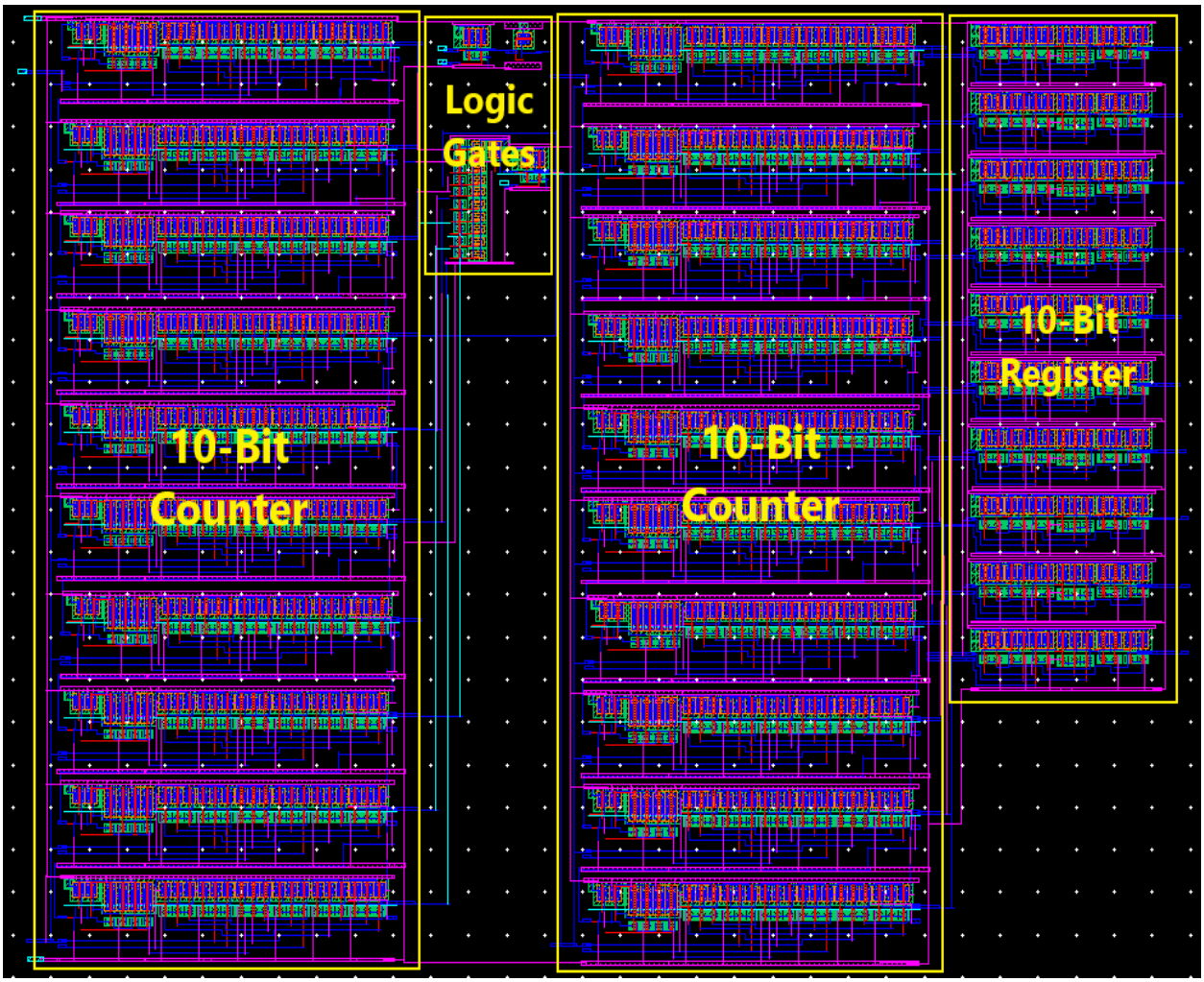


Figure 3.7.2.1: Decimator Layout

3.7.3 Clock Layout

As in the modulator and decimator layouts, we placed the inputs of component blocks near the outputs of the blocks feeding them to avoid signal degradation. The ring oscillator was laid out using two parallel rows of inverters rather than in a long row to avoid having a very long interconnect on one of the nodes. This very long interconnect would have had a larger parasitic capacitance than the other nodes. This asymmetry could cause the oscillator to not oscillate as intended. At the ends of the inverter rows, where the rows had to be connected together with longer interconnects, we used Metal 3 which has a smaller parasitic capacitance per unit length than the Metal 1 used for the other interconnects. This helps to avoid having too large of a capacitance asymmetry in the oscillator. The layout of the clock is shown in Figure 3.7.3.1.

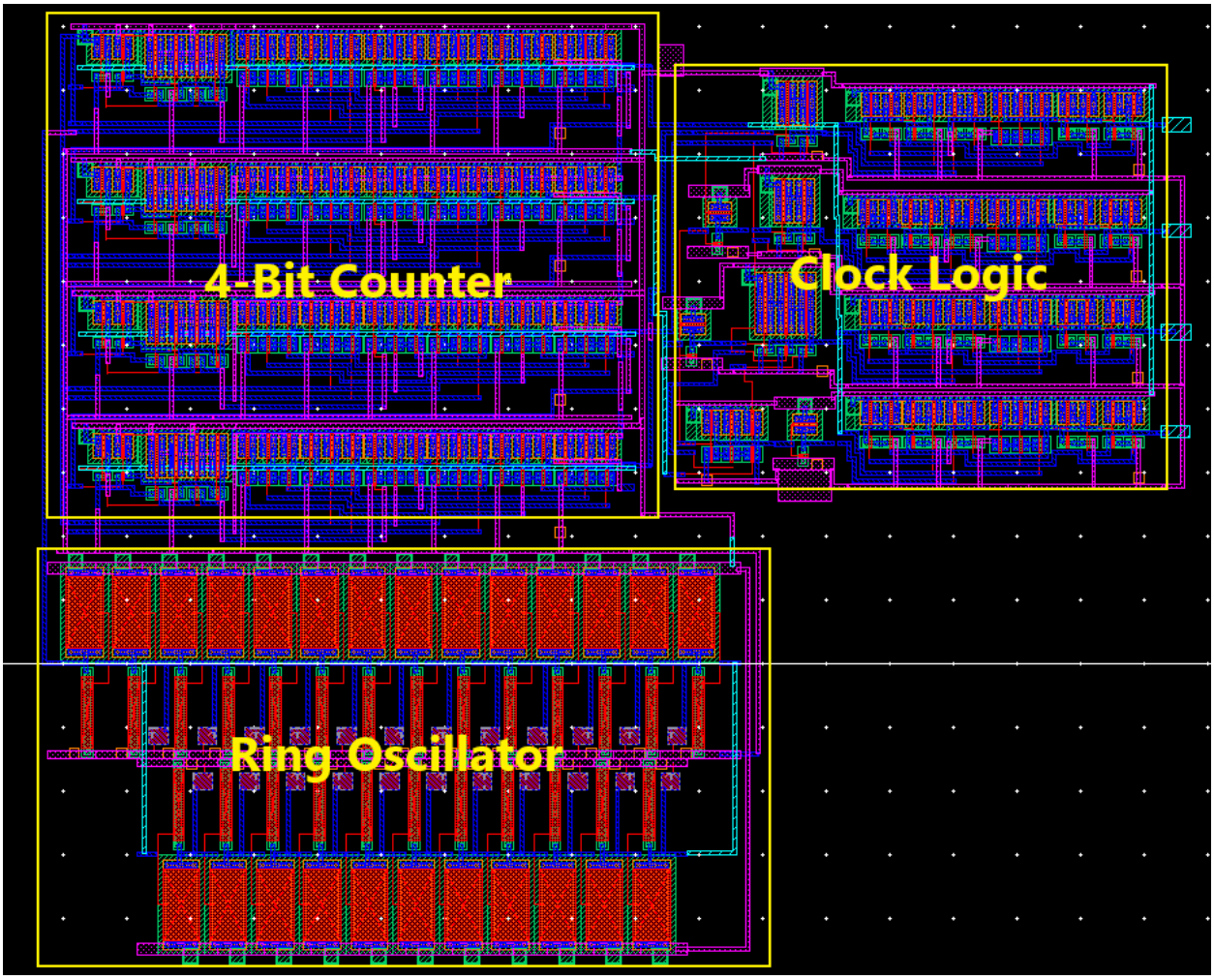


Figure 3.7.3.1: Clock Layout

3.7.4 Temperature Sensor Layout

The main features of the temperature sensor layout differentiating it from the previously discussed layouts are the two serpentine polysilicon resistors. We chose to use polysilicon resistors rather than diffusion resistors because polysilicon has a larger resistance per unit area, higher accuracy, and a lower temperature coefficient. This allows the output characteristics of the temperature sensor to be more linear and closer to the expected characteristics. The layout of the temperature sensor is shown in Figure 3.7.4.1.

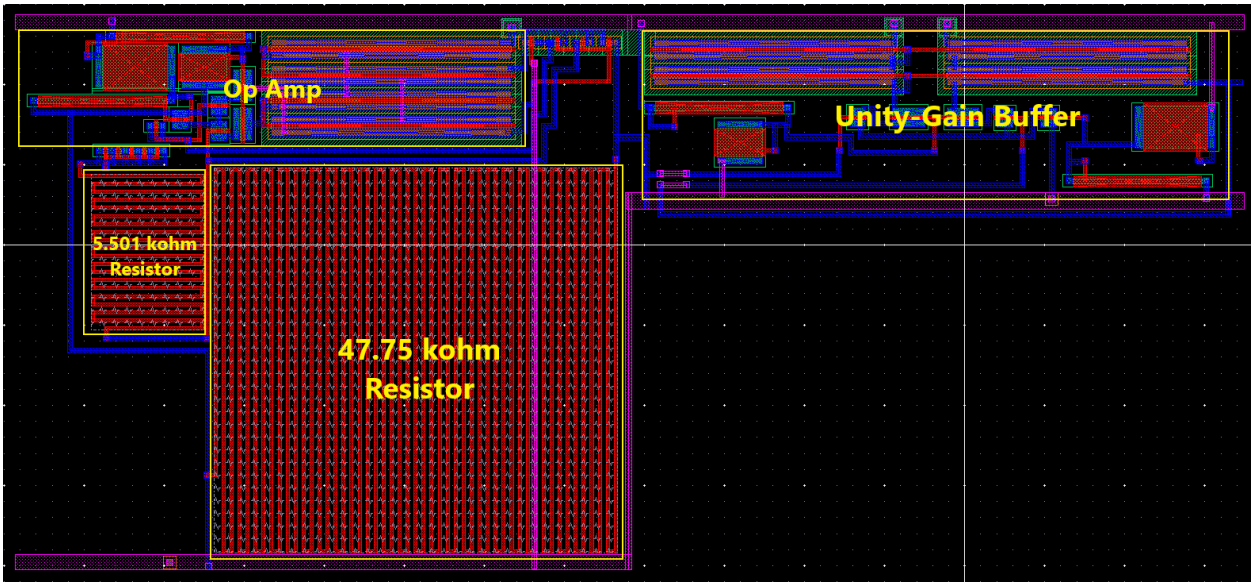


Figure 3.7.4.1: Temperature Sensor Layout

3.8 Pad Frame

Having our circuit fabricated requires a pad frame. The pad frame provides pads where bonding wires can connect the package pins to our circuit's inputs and outputs. Another important feature of a pad frame is ESD protection circuitry. This circuitry consists of a diode and a resistor connected to each pad and serves to protect the circuit from electrostatic discharge through the IC pins. The pad frame that our design was placed in was created by Robert Buckley and Joseph Aymond, two ISU graduate students. The pad frame layout is shown in Figure 3.8.

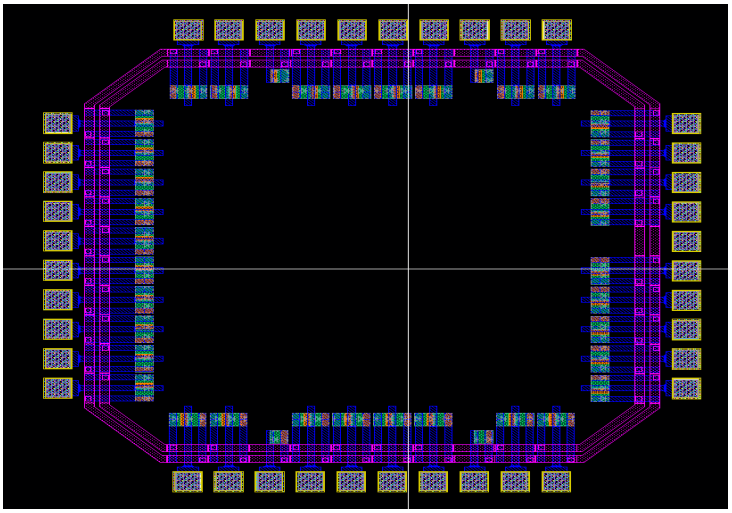


Figure 3.8: Pad Frame

3.9 FABRICATION PROBLEM AND NEW DESIGN

After the physical layout of our 0.18um design was completed, we began preparing to submit our design to MOSIS for fabrication. During this process, we discovered that MOSIS had changed their fabrication policies and would no longer allow 0.18um designs using SCMOS (Scalable CMOS) rules to be fabricated. Since our design was created using SCMOS rules from a 0.18um design kit provided by NCSU, we were not able to have our design fabricated. We investigated the possibility of transferring our design to the native TSMC PDK (Process Design Kit), which would allow fabrication, but we found that we could not use this PDK due to the lack of a legal agreement between TSMC and ISU allowing its use. The only option left for having an ADC design fabricated was recreating our design using the PDK for another process which we could obtain access to. Since there was an agreement between UMC (United Microelectronics Corporation) and ISU to use their 65nm PDK, and there was an upcoming fabrication run of ISU research designs in this process, which had space available for our project, we decided to create a 65nm design and submit it for fabrication.

Since there was only about a six-week window of time in which to complete the 65nm design before the submission deadline, we decided to only include the modulator in the design. This meant that there would be no temperature sensor to use for testing, four clock signals would have to be provided to the chip, and there would be no decimation capability on the chip. This was manageable because an externally generated voltage could be used for testing, our lab equipment could provide the needed clock signals, and software decimation could be used to process the modulator's output.

After reproducing the modulator design in the 65nm process we obtained the physical layout shown in Figure 3.9.1.

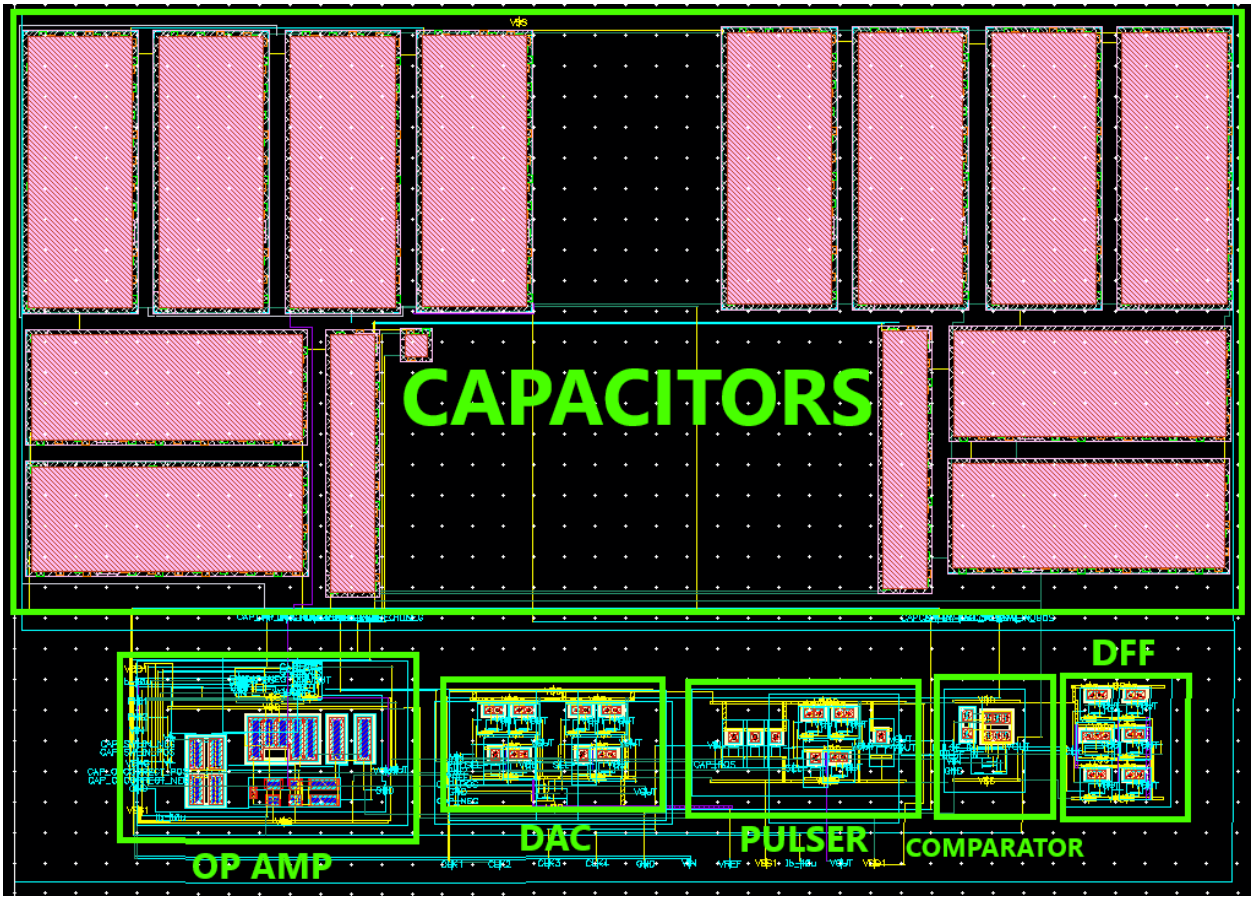


Figure 3.9.1: 65nm Modulator Layout

The pad frame provided to us fit on a 0.5mm x 1mm die and had a core area of 240um x 720 um. Since our layout had an area of only 140um x 200um, there was enough space to fit two of our modulators in the pad frame. We created a modified version of the modulator which had pins connected to test points on the input and output of the comparator and included this with our original design. This would allow us to see the internal operation of the modulator while still maintaining a version with no test points in case the test point connections had an undesired effect on the performance of the circuit. We gated the clocks and added a select signal to choose which modulator would be clocked. This would allow us to measure the power consumption of only a signal modulator while allowing the design to require only 18 pins, less than the 20 pins made available by the pad frame. The full layout with both modulators in the pad frame is shown in Figure. 3.9.2.

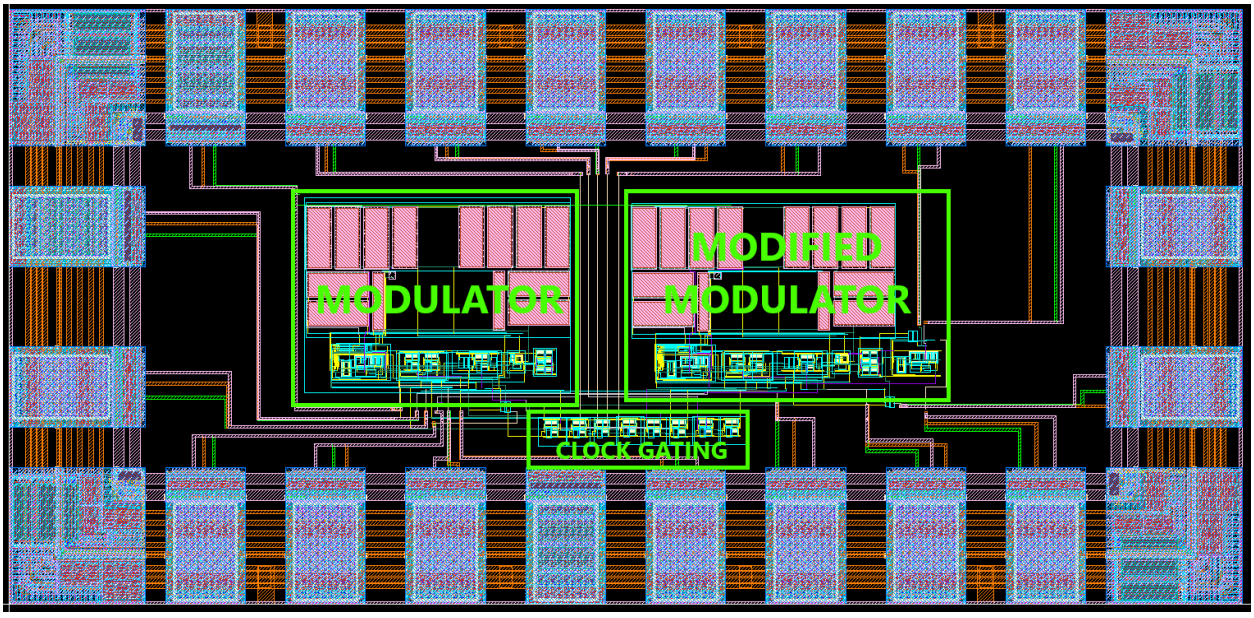


Figure 3.9.2: Full 65nm Layout with Pad Frame

This design was submitted to a joint multi-university project for submission to UMC on Dec. 3rd, 2018. We expect to receive the fabricated chips sometime in February 2019.

4 Testing and Implementation

4.1 Interface Specifications

For the design created in the 180nm process, the input of the ADC should be a voltage in the range of 730mV to 800mV. Reference voltages of 765mV and 800mV should be connected to the appropriate pins. The output of the ADC will be a 10-bit parallel digital signal provided on 10 pins with 0V low voltage and 1.8V high voltage. The output of the temperature sensor will be connected to a pin, which can be connected to the ADC input pin for testing.

For the design created in the 65nm process, it's suggested the user use a voltage reference of 200mV. The input of the ADC should be a voltage in the range of $-V_{ref}$ to V_{ref} (-200mV to 200mV). The output of the ADC will be a binary stream with a -1.25V low voltage and 1.25V high voltage. This binary stream will have to be decimated externally with software as described in Section 5.8 and 5.9.

4.2 Pre-Fabrication Testing

The primary tool that we used for pre-fabrication testing of our ADC and temperature sensor is the Cadence ADE. This software tool is provided by the University for our use on the computers in Coover Hall. The Cadence ADE offers highly accurate design exploration, simulation, and verification for integrated circuits. Using this tool to run simulations allows us to ensure that our circuit will meet our requirements after it is fabricated. To complete the Pre-Fabrication testing for the design created in the 180nm, voltages

were inputted to the ADC modulator and the output codes from the decimator were recorded. This is shown in Table 4.2.4 and the output voltage of modulator is shown in Table 4.2.3.

Cadence was also used to test the ADC designed in the 65nm process this is shown in Figure 4.2.3.1 and Figure 4.2.3.2. Figure 4.2.3.1 shows the voltage inputted into the modulator vs. the corresponding output voltage from the modulator. Figure 4.2.3.2 shows the error of the actual output voltage in comparison to the expected output voltage from the modulator. Alongside those tests the power dissipation was also tested and found to be 224.8µW for the 65nm design.

4.2.1 TEMPERATURE SENSOR

The temperature sensor was tested using Cadence ADE. Simulations were done to verify the monotonicity of the relationship between temperature and output voltage, and to measure the output voltage range corresponding to the 10-degree to 60-degree Celsius temperature range.

The temperature sensor's functionality was tested by sweeping the temperature of the circuit across a range that included the 10 to 60-degree Celsius range of interest and plotting the output voltage. The results are shown in Figure 4.2.1.

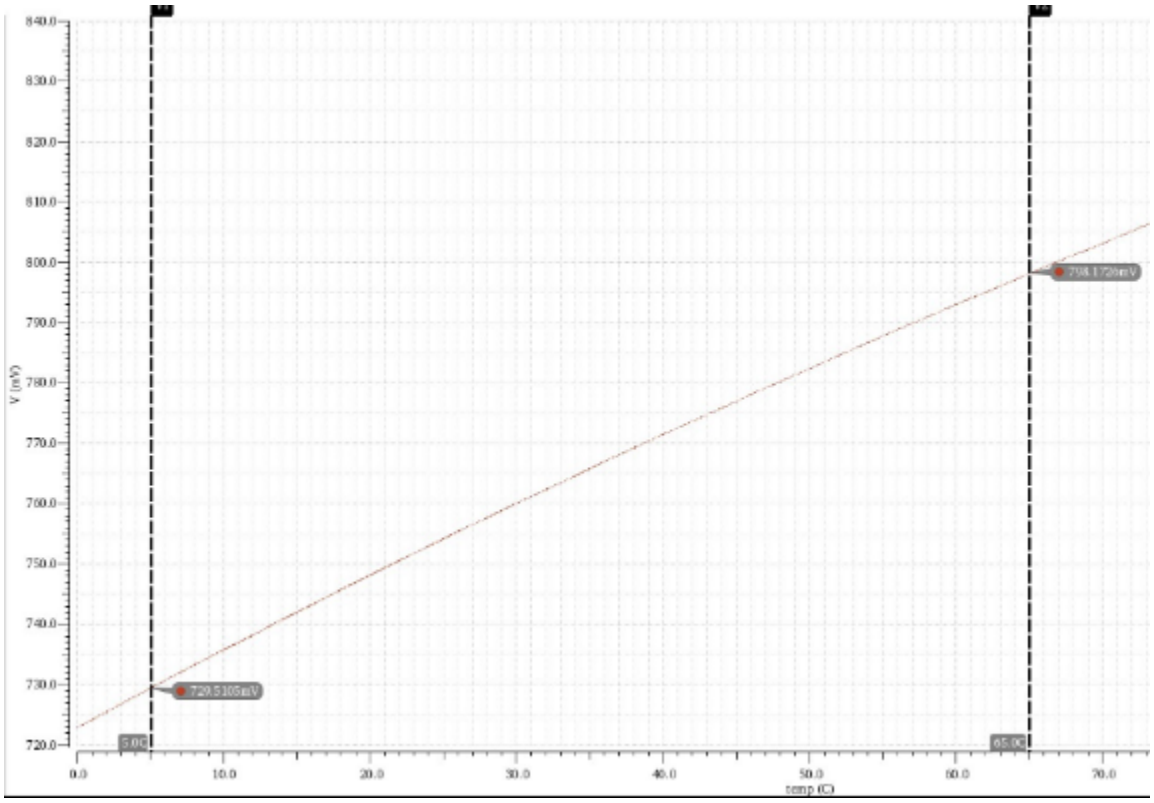


Figure 4.2.1: Temperature Sensor Output

These results verify that the temperature sensor has a monotonic output in the range of interest and operates as intended.

4.2.2 COMPARATOR

The comparator was tested using Cadence ADE. Simulations were done to verify the functionality of the circuit as a comparator, and the input signal swing. The proper input signal swing is necessary to ensure the comparator circuit can react appropriately to the output level of the integrator. The input signal swing range should include the 730mV to 800mV (-200mV to 200mV for the 65nm) range and switching should occur near the center of this range.

We tested the comparator's functionality by applying a gradually increasing voltage to its input and plotting its output. We observed the input voltage, output voltage, and V_{ref} (the trigger point) and saw that the output voltage change was triggered when the input voltage reached V_{ref} as expected (Figure 4.2.2).

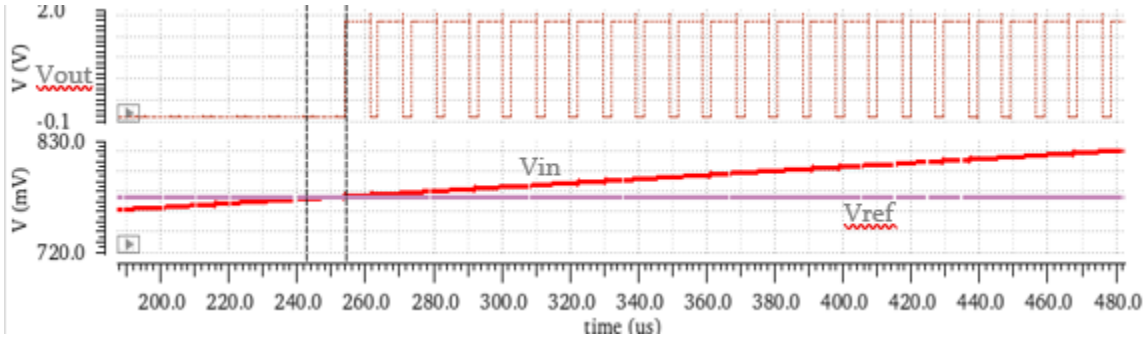


Figure 4.2.2: Comparator Test Results

This verified that the comparator's output voltage changed from low to high when V_{in} exceeded V_{ref}, as intended.

4.2.3 MODULATOR

The modulator was tested using Cadence ADE. Simulations were done to verify the functionality of the circuit. The behavior of the modulator should be that the proportion of the time that the output is high should be equal to the magnitude of the input voltage to the modulator relative to the input voltage range.

The modulator's functionality was tested by connecting the integrator, comparator, and DAC together in feedback configuration. The output of the modulator was then plotted with several input voltages applied to the modulator's input (as shown in Figure 3.5.4.4). An ideal flip-flop was placed at the output to factor out voltage transients. The plotted output was then integrated over a 100ms timespan to obtain a measure for what proportion of the time the output was high. This value was then compared to the expected value to obtain the error. The results for the 180nm design of this testing are given in Table 4.2.3.

Table 4.2.3: Modulator Simulation Results

Input Voltage (mV)	Integrated Value (V*ms)	Expected Integrated Value (V*ms)	Error (%)	Error (V_{LSB})
731	2.724	2.572	0.0844	0.864
747.5	45.105	45.000	0.0583	0.597
765	90.100	90.000	0.0567	0.581
782.5	135.1	135.000	0.0567	0.581
799	177.45	177.420	0.0167	0.171

These results show an error magnitude near the bottom of the input range of between ½ and 1 V_{LSB}, and an error near the top of the range of between 0 and ½ LSB, indicating an effective resolution of around 9 bits.

Similar testing was carried on the 65nm modulator. The 200mV was applied to VREF, causing the input voltage range to be -200mV to 200mV. Voltages covering the entire input range in 10mV increments were applied to VIN and the output of the modulator was integrated over a 10ms time span. This corresponds to one output code of the decimated signal. These integrated values and the error measured as the difference between these and the expected values are plotted in Figures 4.2.3.1 and 4.2.3.2.

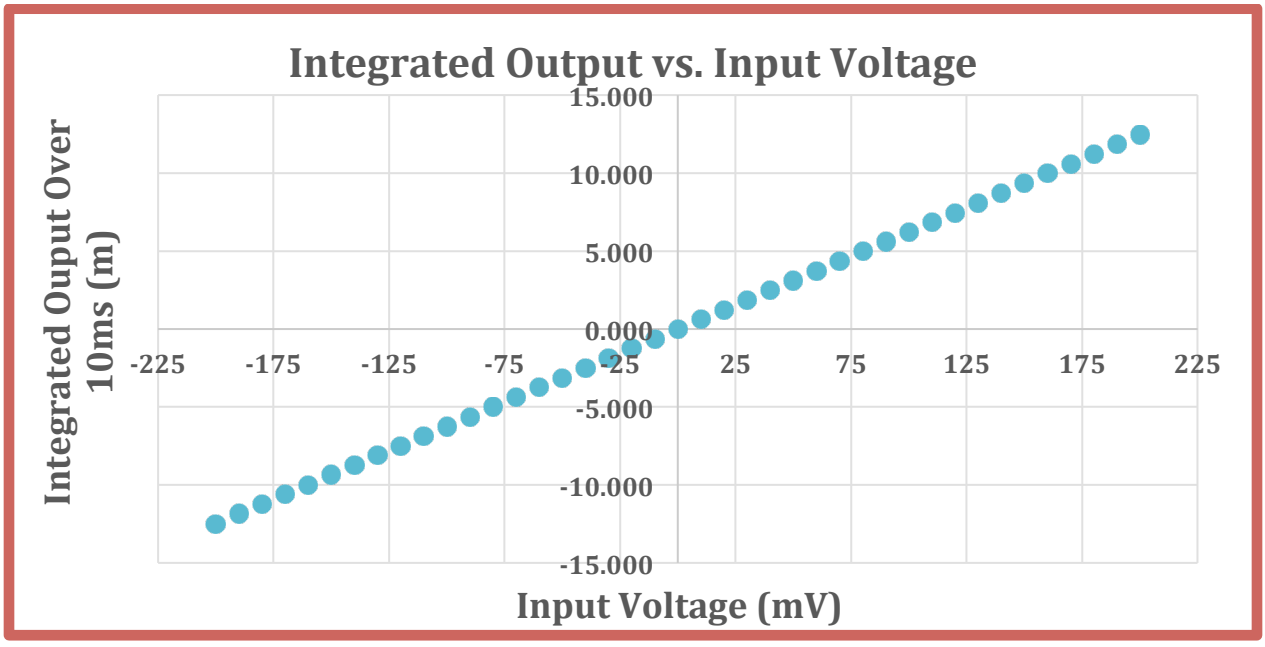


Figure 4.2.3.1: Integrated Modulator Output vs. Input Voltage

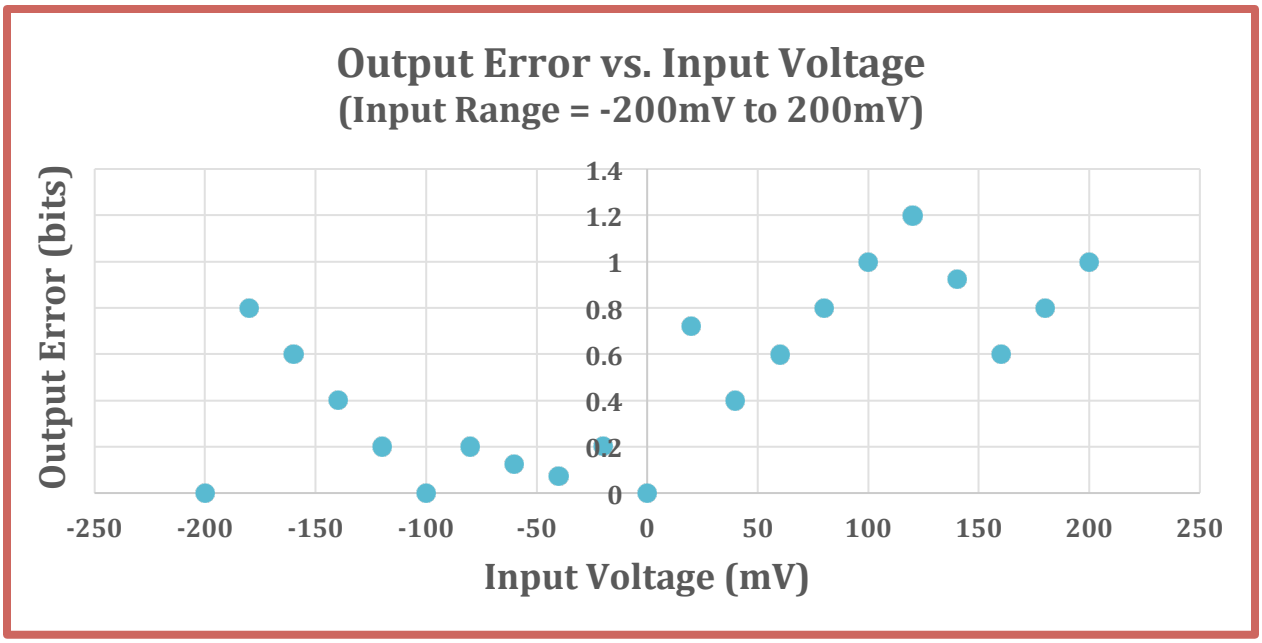


Figure 4.2.3.2: Output Error vs. Input Voltage

These results show that the error is at most 1.2 bits, indicating an effective resolution of around 9 bits.

4.2.4 Digital Decimator

The Digital Decimator is only included in the 180nm design. The decimator was tested using Cadence ADE. Simulations were done to verify the functionality of the circuit. The behavior of the decimator should be that it outputs a 10-bit code on its 10 parallel output pins whose magnitude is proportional to the proportion of the input values that are high in a 10ms timespan. A new code should appear at the output once every 10ms.

The decimator's functionality was tested by connecting the output of the modulator to its input and observing the decimator's output codes with several input voltages applied to the modulator. Two output codes were collected at each voltage.

The results of this testing are given in Table 4.2.4.

Table 4.2.4: Decimator Simulation Results

Input Voltage (mV)	First Code	Second Code	Expected Code
730.068359375	3	2	1
752.5	257	256	256
765	512	512	512
782.5	767	767	768
799.931640625	1023	1023	1023

These results show that the output code of the decimator with the modulator connected to its input varies by no more than 2 LSBs from the expected code.

4.3 Post-Fabrication Testing

IEEE standards will be followed during testing of the delta-sigma data converter. The standard that will be used is the IEEE Standard for Terminology and Test Methods for Analog to Digital Converters[7]. This standard outlines testing methods that will allow us to characterize the data converter and determine the quality of its functionality. The Post-Fabrication testing can be applied to both the 65nm and the 180nm design.

Testing the physical IC after fabrication will require the use of a digital multimeter or oscilloscope to measure voltages, DC power supplies to provide bias voltages, and an oven or dielectric bath to control chip temperature. We will also require anti-static wrist straps to avoid destroying our ICs through accidental electrostatic discharge. All this equipment is available to us in the labs in Coover Hall.

In addition to this standard lab equipment, we will also acquire two DAQs that will allow the 10-bit parallel output of the ADC to be read by a computer. Initial testing will be on the MCC USB-201 and final testing on the MCC USB-1208HS. These DAQs will interact with DAQami software from Measurement Computing.

Initial testing will be on the MCC USB-201 and final testing on the MCC USB-1208HS. The USB-201 does not have the same number of inputs pins as our ADC's output pins, thus we will need to truncate our output data from the ADC for initial testing which may introduce measurement error. For the initial tests, only basic conversion and characteristics will be tested rather than spectral characteristics of the design. Following the initial testing the USB-1208HS will be used to focus on the spectral characteristic of the ADC, and it will be used to complete any final necessary testing.

The USB-201 model is desirable because we currently have access to this model. It meets most specifications except for number of channels and input sample speed. Our design is faster than this model specifies since our design is a high-speed architecture. In addition this model does not contain the correct number of I/O so that we can properly read our output data.The USB-1208HS meets all the specifications that the USB-201 does not, but we do not have current access to the DAQ. This DAQ is not necessary for the initial testing, thus we can begin testing with the model that we currently have available and still produce sufficient results.

The DAQ will gather the output codes of the ADC in relation to the input analog voltage; this data will be imported into a computer through DAQami software. The DAQami software from MCC provides us with access to a .CSV file, which would be sent to MATLAB for post-processing of our data. The DAQami software has an interface to receive data from both USB-201 and the USB-1208HS, and allow us to send signals back to our ADC if needed. This data will be manipulated using MATLAB to produce valuable test results.

The parameters that are specifically tested will be outlined in the next sections. The chip will be fabricated as a 20-pin dip. We will connect the fabricated chip into a PCB; this will simplify the connection between the DAQ and the ADC.

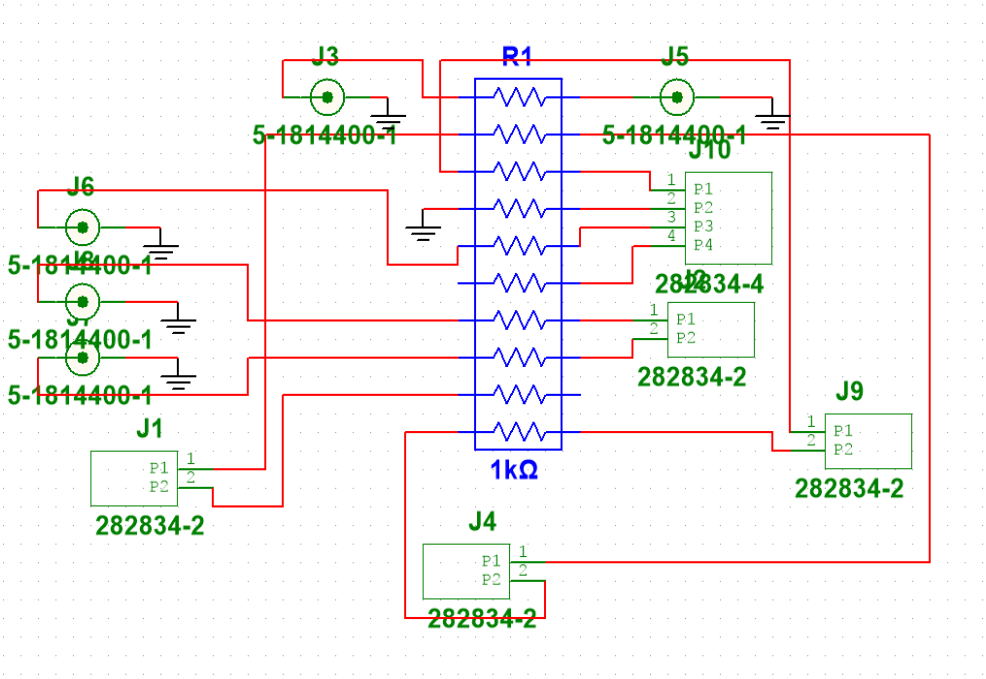


Figure 4.3.0.1 PCB Schematic

In order to perform basic testing we will need to provide jumpers from individual pins so that we can provide external voltages, and output on jumper pin. Shown above our chip, which is a 20-pin, DIP is modeled as a 20-pin DIP of 10 1k resistors. The ADC will be put into that same package and socket. The software used for design does not have a 10-pin jumper so an 8-pin and 2-pin was used instead.

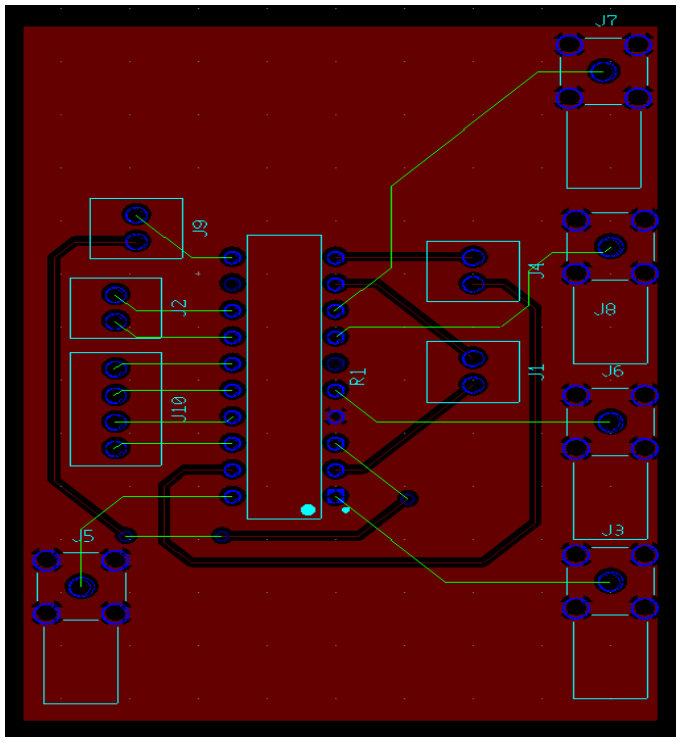


Figure 4.3.0.2 PCB Layout

4.3.1 INL/DNL

INL and DNL are not typically reported with a Delta-Sigma ADC. The oversampling and feedback gives us higher resolution, but the input must go through an integrator, comparator, and a decimator before the digital code is acquired out the output. It is very difficult to define a deterministic latency between the analog input and the digital output code. It is possible to define these terms using a very large number of input samples, but generally SNDR, SNR, and SFDR provide all of the essential performance information. Regardless the INL provides information regarding the difference between the midpoints of the quantization steps between the ideal and the real transfer function.

$$\boldsymbol{INL = Voltage\ midpoint\ ideal - Voltage\ midpoint\ actual} \quad (4.3.1.1)$$

The DNL measurement provides information regarding the difference between the ideal step-width and the actual step-width.

$$\boldsymbol{DNL = \frac{Voltage_{k+1} - Voltage_k}{Voltage_{Ideal\ LSB}} - 1} \quad (4.3.1.2)$$

4.3.2 SNR

To calculate the Signal-to-Noise Ratio (SNR), we use the following equation:

$$SNR = \frac{A_1^2}{\sqrt{\sum_{k=0}^{\infty} N_k}} \quad (4.3.2)$$

Where A1 is the magnitude of the fundamental on the output and Nk is the magnitude of the noise floor at each remaining frequency (not including the noise at the harmonic frequencies). We will determine the magnitude of these values by taking the DFT of the output once we have the data imported into our computer.

4.3.3 SNDR

To calculate the Signal-to-Noise and Distortion Ratio (SNDR), we use the following equation:

$$SNDR = \frac{A_1^2}{\sqrt{\sum_{k=0}^{\infty} N_k}} \quad (4.3.3)$$

This is similar to the calculation for SNR, except here we include the magnitude of the noise floor at each of the harmonic frequencies in addition to all of the non-harmonic frequencies. Again, the DFT of the output will be taken once imported into the computer. We can then use Microsoft Excel to implement a simple formula on our imported data to give us the resulting SNDR.

4.3.4 ENOB

Because INL and DNL aren't normally reported for a Delta-Sigma ADC, we may use the SNDR to calculate the Effective Number of Bits (ENOB). ENOB will tell us how high the actual resolution of our data converter is in comparison to what we were expecting. The following equation may be used to find the ENOB:

$$ENOB = \frac{SNDR - 1.76\ dB}{6.02} \tag{4.3.4}$$

We divide by a factor of 6.02 to convert decibels (log10) to bits (log2). The subtraction of 1.76 dB is the quantization error in an ideal ADC.

4.3.5 MATLAB PROCESSING

Obtain the output waveform from the ADC using the DAQ, the DAQ will then format the transition points into a .CSV file. There should exist $2^{10} - 1$ transition points.

Using this output waveform we can obtain the FFT of the signal and solve for THD and SNR. The FFT is created in Matlab with the following code:

```
%Where data is set to the data inputted from the .csv file
Filename = 'mcc_data.csv';
 data=csvread(filename,r1,c1);
%r1=0,c1=0 is default case where we read from the first value in the file
Fs = 1024000; %sampling frequency
N = 2^10; %number of sampling points
Ts = 1/Fs;
t = 0 :Ts: (N-1)*Ts %sampling time array
spec=(fftshift(fft(data,length(data))/length(data)));
freq=(-length(data)/2:length(data)/2-1)*fs/length(data);
figure(1);
plot(freq,db(abs(spec)));
%A Blackman window may provide a more accurate result due to incoherent sampling
 %Change in the sampling window can result in error with fundamental frequencies and
harmonics
%The better the windowing technique  the error occurs at a higher bit level blackman
shouldn't have errors until the 13th bit
M = blackman window length;
N= FFT length;
W= blackman(M);
X= output waveform; %data from .csv file
XW = [W.*X , zeros(1, zpf-1)*M)];
figure(2);
plot(XW);
V = abs ((fft(data, N)))/N;
V = V/max(V); %normalizing the spectrum
V_db = db(V);
V_2 = v(1: N/2);
```

```
[Vs,is] = max(v(1: N/2));
Power = Vs^2; %fundamental signal
Pharmonic = norm(V_2(2 - is-1))^2 +norm(v_2(is+1:N/2))^2 %harmonic power
Pnoise = norm(V_2(find (db(V_2 < -300)))^2
SNR = 10*log10(Power/Pharmonic);
SNDR =10 *log10(Power/Pnoise);
```

If the number of periods of the sampled signal periods is not an integer the Fourier coefficients are non-zero at harmonics; this concept refers to spectral leakage.

4.3.6 Power on timing

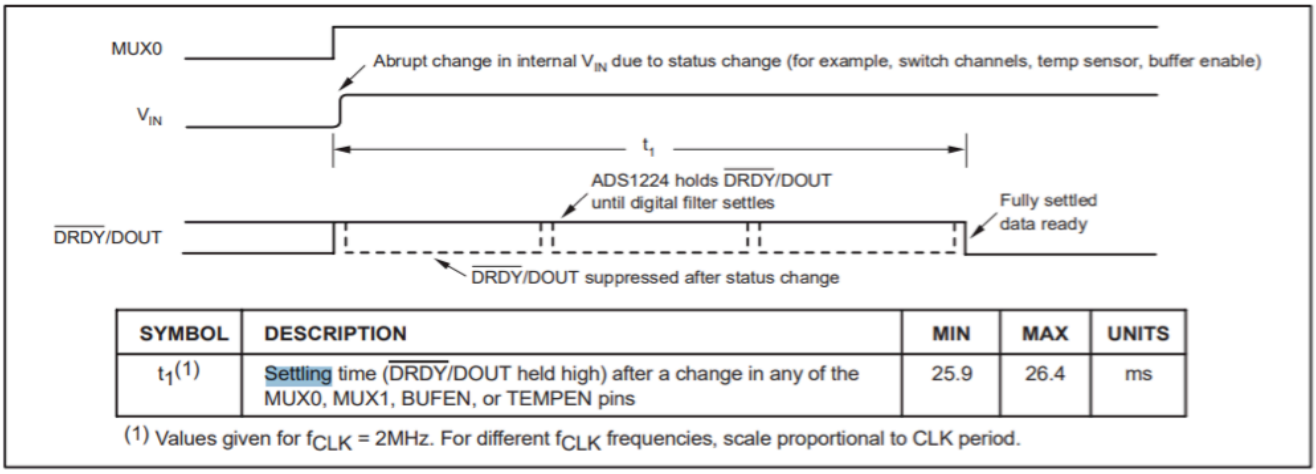
Purpose: To ensure that our device is available within a viable length of time, and how long the user must wait before being able to receive accurate data.

1. Start with a known value for settling time. Example value could be the transition from an output of 500 to an output of 512.
2. Power down the device. Remove all power for at least 5 seconds.
3. Power on the device.
4. Take measurements for the change in time from a known value to a changed value. In the example start with power off and an initial data point of 500. When power is introduced also change the analog input to the equivalent of 512.
5. Subtract this measurement with the known value to receive a value for power on timing.

4.3.7 Settling Time

Purpose: To ensure that data will reach a steady state. To verify that output data codes will be accurate within a reasonable amount of time. Ensure smooth transitions between analog inputs.

1. Start with a steady state. Power is on, no change in output for over 3 seconds, and a known initial analog value. Example start with 500 digital values from an analog input.
2. Change the analog value to transition to a value, which is of substantial distance from the initial value so as to verify a transition has occurred. Example: end with 512 digital outputs from an analog input of equivalent value.
3. Measure output as it stays constant for greater than a set amount of cycles. This amount could be 3 to verify that the device has not overshot the target data.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_1(1)	Settling time ($\overline{DRDY}$/DOUT held high) after a change in any of the MUX0, MUX1, BUFEN, or TEMPEN pins	25.9	26.4	ms

(1) Values given for f_{CLK} = 2MHz. For different f_{CLK} frequencies, scale proportional to CLK period.

Figure 4.3.7: Settling Time Graph

4.3.8 Output data rate

Purpose: Compare the expected data rate of our output with actual measured values. This is one test to verify the accuracy of the fabrication process. Will give a set of data, which shows variation between the same design, and different chips.

1. Set the analog value to a known digital value. An example could be the digital value 500.
2. Wait for data output to stay steady for a set amount of cycles, for example 3.
3. Sweep the analog data value over an array of values. An example would be to increase by 1 from 500 up to 1000.

4.3.9 Power consuption

Purpose: Measure static power consumption for the output data, for a given input. Determine how much power draw this device will take, and if that will be prohibitive to the feasibility of our eventual design.

1. Implement a shunt resistor on input V_{DD} to read the voltage drop and current drawn over a small resistance. Example resistance might be of the magnitude 3.3 ohms.
2. Calculate power draw from that set resistance, and the input voltages and current drawn.

4.3.10 Output delay from input signal

Purpose: Measure delay through our design. Determine the critical timing in our design. Determine whether delay is a prohibitive factor to our design.

1. Utilize a known analog value on input. Example input value could be the equivalent of digital value 500. At the time that input analog signal is set to a settled time read as time, t=0.
2. Take another known analog value for input. Example input value could be the equivalent of digital value 512.
3. Record the known clock frequency.
4. Change to this new analog value.
5. Measure the time that it takes for the FIRST digital output code of 512 to occur on the output.
6. Calculate the number of clock signals given the known clock frequency and measured time.

4.3.11 Temperature Sensor

After fabrication, the temperature sensor will be tested with one of two methods. The first is with an oven in the VLSI lab in Coover Hall. The chip will be placed on a breadboard, which will be placed in an oven. A multimeter probe will be connected to the temperature sensor's output pin through the porthole in the oven. The oven's temperature will then set to a variety of temperatures within the 10 to 60-degree Celsius range. At each temperature, the sensor's output voltage will be measured with the multimeter and recorded. These measurements will then be compared with the Cadence simulation results. If this testing method fails to give consistent results when taking measurements at the same temperature multiple times, the second method will be used.

The second method for testing the temperature sensor is to emerge the IC in an electrolytic bath. The bath consists of a vessel containing an electrolytic liquid, which is heated to a well-controlled temperature. The output voltage will then be measured with a multimeter probe at a variety of temperatures.

4.4 Implementation and Testing Challenges

The primary challenges that we have had in the implementation and testing of our circuit are the short amount of time that we have available to build our circuit, and the long periods of time required to run Cadence simulations on our complete circuit.

The long periods of time that it takes to run Cadence simulations on our complete circuit has made it difficult to test the effects of small changes on the performance of our complete circuit. One way we have mitigated the effects of this problem by testing only one segment of our circuit at a time to measure its performance as its design is being improved. This allows simulations to run more quickly because fewer circuit nodes need to have calculations done for them. Another way we have mitigated the effects of this problem are by running simulations using ideal clock sources rather than the clock that we built. This allows for a significant reduction in simulation time due to the elimination of the need to perform large numbers of calculations on the nodes of the ring oscillator in the clock.

Another large challenge we came across that is also mentioned in section 3.9, is the issue of not being able to fabricate in the 180nm and switching over to the 65nm process. This required us to understand the new design rules that came along with the 65nm process. We were also once again constrained by time to finish the design to fabricate as soon as possible.

4.5 Nonfunctional Requirements

The preceding sections of Part 4 have discussed implementation and testing for the functional requirements of our project, which are all but one of the requirements. The only non-functional requirement is that the circuit layout dimensions not exceed 4 millimeters by 4 millimeters. Our circuit has an area of 180um x 240um. This is much smaller than our allowed area, which will allow our ADC to be integrated in other ICs without consuming a significant amount of die space.

5 User's Guide

5.1 Pin Layout

The layout of the pins for the fabricated IC package is as shown in Figure 5.1. Care should be taken to ensure correct orientation of the marker dot to properly identify pins relative to the diagram.

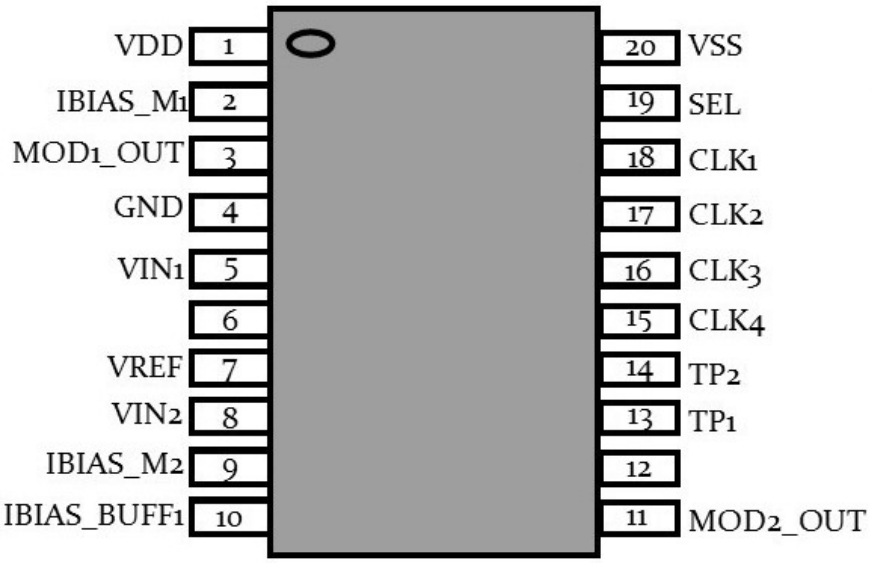


Figure 5.1: Chip Pin Layout

5.2 Necessary Precautions

This chip contains delicate circuitry and the ESD protection provided by the pad frame may be less than ideal. Therefore, proper precautions should be taken to avoid damage to the chip due to electrostatic discharge (ESD).

Handling of the chip should only take place by a person wearing an ESD protection wrist strap that is properly grounded. This will prevent static charge from building up on the person's body which can discharge to the chip. Additional precautions that can be taken to reduce the risk of ESD damage are using an ESD protective tray under the chip, an ESD protective table top as a work area, and an ESD protective floor or mat (Figure 5.2).

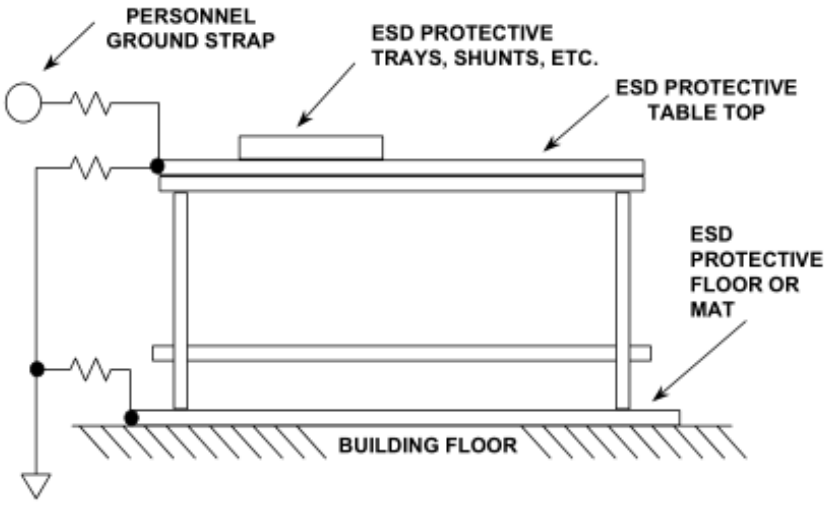


Figure 5.2: ESD Protective Equipment[10]

Care should also be taken to only connect equipment to the chip, which will not apply large voltage, or current spikes to the chip.

5.3 Interfacing with the Chip

The IC is housed in a standard 20-pin DIP package. The IC should only be interfaced with by placing it in a socket compatible with this type of package. This socket can be attached to a PCB that can route the necessary signals and supplies to the correct pins.

5.4 Connecting Power Supplies

The chip is designed to operate at VDD = 1.25V and VSS = -1.25V. These voltages should be applied to the indicated pins using stable voltage supplies, which can supply currents of at least 90uA continuously with spikes of up to 7mA. The GND pin should be connected to 0V.

5.5 Selecting and biasing the Modulator

The chip contains two modulators. One standard modulator (MOD1), and one testing modulator (MOD2). MOD2 is the same as MOD1, except with test points added to the input and output of the comparator. These test points are connected through buffers to pins TP1 and TP2 respectively. If test point voltages do not need to be observed, MOD1 should be used to exclude the presence of parasitics introduced by the test point connections.

Only one modulator can be used at a time. To use MOD1, apply -1.25V to the SEL pin. To use MOD2, apply 1.25V to the SEL pin. Depending on which modulator is being used, a 10uA biasing current must be applied to either the IBIAS_M1 or IBIAS_M2 pin to bias the op amps on the chip. If MOD2 is being used, an additional 10uA biasing current must be applied to the IBIAS_BUFF1 pin to bias the TP1 output buffer. These biasing currents should be supplied by a stable and accurate current source.

5.6 Clocking the Modulator

The modulator is designed to operate with four synchronized clock signals applied to pins CLK1, CLK2, CLK3, and CLK4. These clocks should have low voltages of -1.25V and the high voltages of 1.25V. Their phases and duty cycles are given in Table 5.5.

	Phase	Duty Cycle
CLK1	0°	1/4
CLK2	180°	1/4
CLK3	180°	1/8
CLK4	315°	1/8

Figure 5.6: Clock Phases and Duty Cycles

The modulator is designed to be used with a clock frequency of 102.4kHz. Other clock frequencies may be possible, but results are not guaranteed since simulations have not been performed at other frequencies.

5.7 Setting the Input

The analog input signal voltage should be applied to the VIN1 or VIN2 pin depending on the modulator being used. The signal source should be capable of driving up to 500uA of current without distorting the signal. If this isn't possible, an analog buffer created with an op amp as shown in Figure 5.6 should be placed between the signal source and the VIN pin being used. This buffer could also be used to increase the input resistance of the modulator if needed.

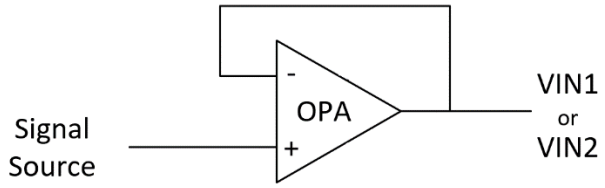


Figure 5.7: Analog Buffer

A reference voltage should be applied to the VREF pin as appropriate for the voltage range of the input signal source. The input signal range of the modulator will be -VREF to +VREF. Testing was carried out with VREF = 200mV, so results using other reference voltages may differ from those obtained from our tests. The reference voltage should be applied from an accurate and stable voltage source. The accuracy of the modulator's output is limited to that of the reference voltage applied.

5.8 Reading the Output

The modulator produces a binary bit stream at either MOD1_OUT or MOD2_out, which must be read using a data acquisition unit (DAQ). The bit stream has a low voltage of -1.25V and a high voltage of 1.25V, so the DAQ's sensitivity must be set accordingly. The bit stream's frequency is equal to the frequency of the modulator clocks, so the DAQ can be triggered using one of these clocks.

5.9 Processing Output Data

The output data needs to be decimated to produce a useful output value. Adding a fixed number of output bits to produce each output code does this. Using a higher OSR will generally produce higher resolution at a cost of output value frequency. The recommended OSR to use is 1024. This corresponds to one output code being produced every 10ms at nominal clock frequency (102.4kHz). Using this OSR, MATLAB or other suitable software must be used to add each successive string of 1024 bits to produce each successive output code. This produces output values with 10 bits of resolution. The voltage corresponding to each output code can be calculated with equation 5.8.

$$Corresponding\_Input\_Voltage = 2 * \frac{VREF}{OSR} * Output\_Code - VREF \quad (5.8)$$

6 Closing Material

6.1 Closing Summary

The goal of our project was to design a high-resolution data converter IC that converts analog voltage to a digital representation. The data converter is implemented along with a temperature sensor in a single chip to allow the chip's temperature to be communicated as a digital signal. The accurate high-resolution temperature measurement can be used to trigger the chip to throttle its operation to prevent overheating. After researching ADC architectures, we decided to use a specific delta-sigma ADC architecture to realize our IC for its high accuracy, low power consumption, and simplicity. Our IC has 10-bits of resolution and measures a temperature range from 10C to 60C with an oversampling ratio of 1024 to 1, which means that for every 1024 samples taken at the input, one sample will be asserted at the output. The delta-sigma ADC is comprised of several functional blocks. All these blocks have been designed at the transistor level and have been tested individually and combined to ensure that the product will be functional after fabrication.

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